A5931

Three Phase Sensorless Fan Driver

FEATURES AND BENEFITS

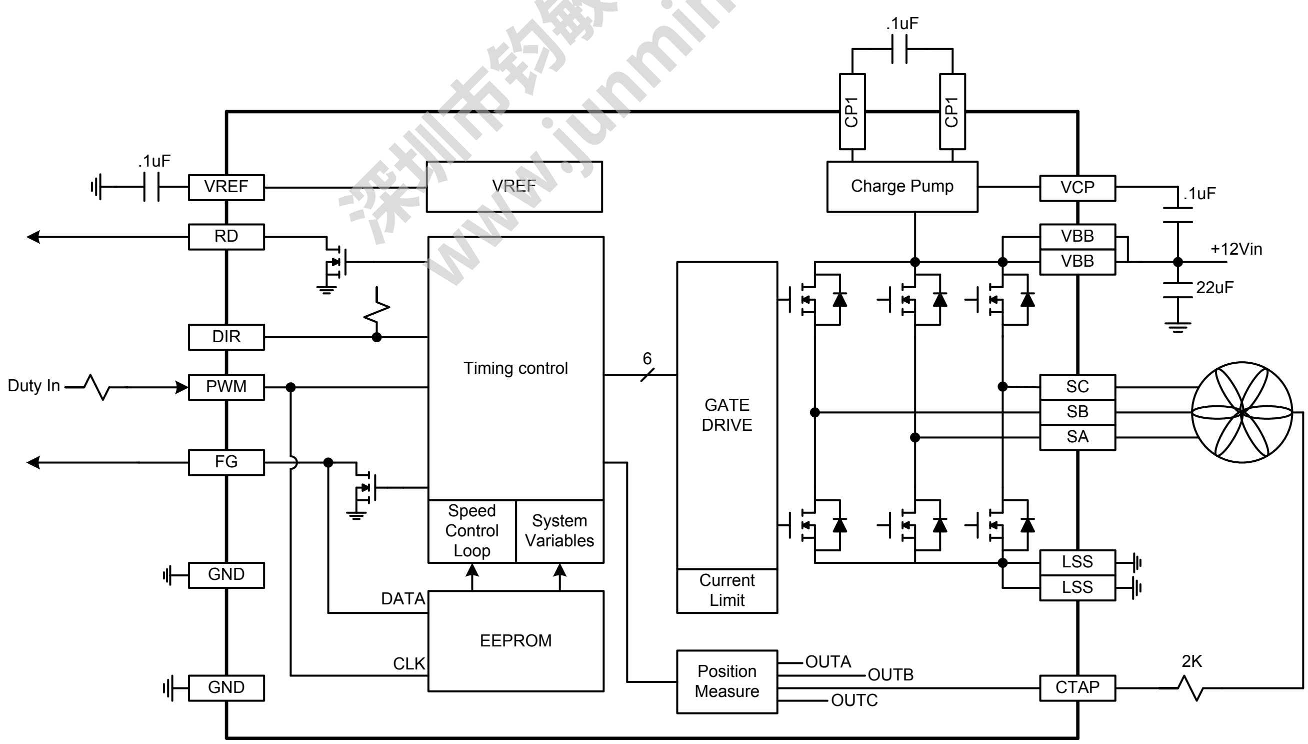
- Closed Loop Speed Control
- Speed Curve Configuration via EEPROM
- I2C Serial port
- Sinusoidal modulation for Reduced Audible Noise and Low vibration
- Sensorless (No Hall Sensors required)
- Low RDSON Power MOSFETs – 3A capability
- Minimal External Components
- PWM Speed Input
- FG Speed Output
- RD Rotor Lock Output
- Lock Detection
- Soft Start
- Standby Mode
- Overcurrent Protection

DESCRIPTION

The A5931 three phase motor driver incorporates Sensorless sinusoidal drive to minimize vibration for high speed server fans. Sensorless control eliminates the requirement for hall sensors for server Fan applications.

A Flexible Closed loop speed control system is integrated into the IC. EEPROM is used to tailor the common functions of the fan speed curve to a specific application. This eliminates the requirement for a microprocessor based system and minimizes programming requirements.

The A5931 is available in a 24L 4x4 QFN with exposed power pad, (suffix ES), and a 16L SOIC with exposed power pad (suffix LP).



Typical Application

Table of Contents

Selection Guide

Part Number	Packing	Package
A5931GES		
A5931GLP		

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}	DC			18	V
		Tw<10ms			20	V
Logic Input Voltage Range	V_{IN}	SPD, DIR	-.3		6	V
Logic Output	Vo	FG, RD			V_{BB}	V
Output Current	I_{OUT}				Internally Limited	A
Output Voltage					$V_{BB}+1$	V
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta		-40		105	°C
Package Thermal Resistance						
A5931GES	Rja	2 sided PCB 1 in^2 Copper		45		°C/W
A5931GLP		2 sided PCB 1 in^2 Copper		35		

Recommended Operational Range

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}	DC	5	12	16	V
Logic Input Voltage Range	V_{IN}	PWM	-.3		6	V
Motor Current	I_{OUT}	Sinusoidal Running Mode			3000	mA

Terminal List

Pin Name	Pin Description	ES	LP
FG	Output Signal	1	6
SPD	Logic Input – Speed Demand	2	7
RD	Logic Output Signal	3	8
DIR	Logic Input	4	-
n/c	No connect	5	-
LSS	Low Side Source connection	6	9
OUTA	Motor Terminal	7	10
VBB	Input Supply	8	11
OUTB	Motor Terminal	9	12
n/c	No connect	10	-
VBB	Input Supply	11	13
OUTC	Motor Terminal	12	14
LSS	Low Side Source connection	13	15
VCP	Charge Pump Capacitor	14	16
CP2	Charge Pump Capacitor	15	1
CP1	Charge Pump Capacitor	16	2
n/c	No connect	17	-
n/c	No connect	18	-
VREF	Reference Voltage Output	19	3
n/c	No connect	20	-
CTAP	Motor Terminal	21	4
n/c	No connect	22	-
GND	Ground	23	5
n/c	No connect	24	-

Electrical Characteristics
A5931Gxx at TA = +25°C, VBB = 5V to 16V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	IBB	Active Mode (PWM duty < DC_ON)		8.5	13	mA
	IBBS	VBB=12V, Standby Mode			50	uA
VREF	V_{REF}	I=0ma to 10mA	2.7	2.8	2.9	V
Power Driver						
Total Driver Rdson (Sink + Source)	RDSON	I = 1.5A, Tj=25C, VBB=12V		210	250	Ω
		Source Driver		105		mΩ
		Sink Driver		105		mΩ
Motor PWM Frequency	f_{PWM}		23.4	24.4	25.4	kHz
Speed Control						
PWM Duty Input			.1		100	kHz
Duty Cycle On Threshold	DC_{ON}	Relative to target	-.5		.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to target	-.5		.5	%
SPD Standby Threshold (Analog)	SPD_{TH}			.7	.8	V
SPD On threshold	SPD_{ON}	DCON = 10%	220	250	280	mV
SPD On threshold	SPD_{OFF}	DCOFF = 8%	170	200	230	mV
SPD Max	SPD_{MAX}			2.5		V
SPD ADC Resolution				4.89		mV
SPD ADC Accuracy		SPD = .2V to 2.5V		+/-6		LSB
Speed Setpoint	F_{SPD}		-5		5	%
Protection Circuits						
Lock Protection	t_{OFF}	Relative to target	-10		10	%
VBB UVLO	VBB_{UVLO}	VBB rising		4.4		V
VBB UVLO HYS	VBB_{HYS}		160	300	480	mV
OverCurrent Protection	I_{OCP}			5		A
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing.	150	165	180	°C
Thermal Shutdown Hysteresis	ΔTJ	Recovery = T_{JTSD} - ΔTJ		20		°C

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization

A5931Gxx at TA = +25°C, VBB = 5V to 18V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Logic/Input Output/I2C						
Logic Input Low Level	V_{IL}		.8			V
Logic Input High Level	V_{IH}				2	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mv
Logic Input Current	Iin	SPD	-10	<1	10	uA
		DIR, VIN=0V, 100K Pull Up		28		uA
Output Sat Voltage (FG,RD)	V_{SAT}	I=5mA			.3	V
Output Leakage (FG,RD)	I_O	V=16V, Switch OFF			1	uA
I2C timing						
SCL Clock Frequency	f_{CLK}		3	–	400	kHz
Bus Free Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	µs

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization

Functional Description

The A5931 targets high speed fan applications to meet the objectives of minimal vibration, high efficiency, and ability to customize the IC to the speed control specification.

In typical systems, an MCU is required to meet each application spec. The A5931 integrates the basic closed loop speed control function, thus allowing elimination of the cost, pcb space, and programming requirements of a custom MCU.

For each specific application the EEPROM settings can be created with the Allegro EVB and software. Contact Allegro sales to order the custom IC. (Minimum volume requirements will apply).

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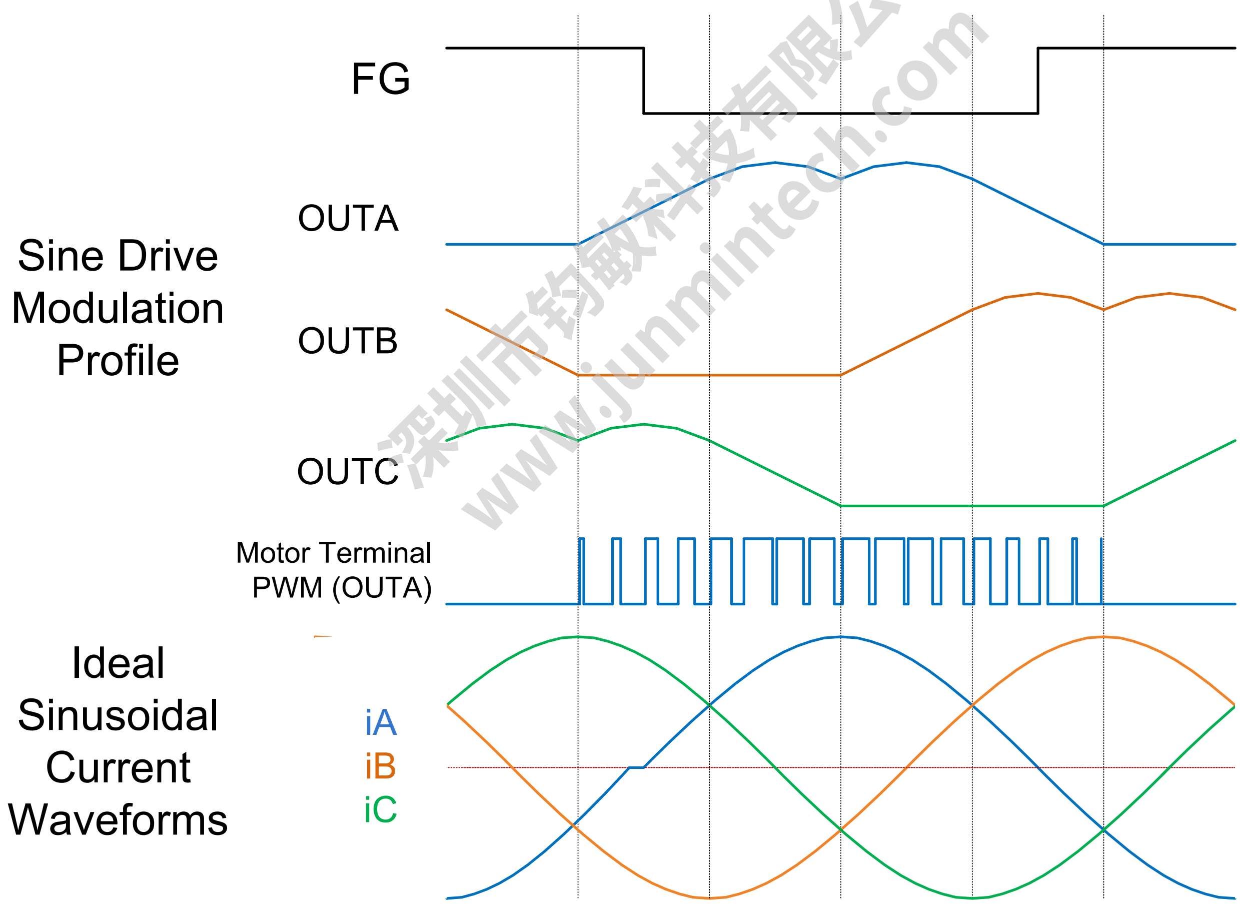
The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 9bit number. This 9 bit “demand” is translated to a speed signal based on settings that are configured via EEPROM.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

Standby mode can be achieved by holding SPD pin low for longer than the programmed Lock off-time. In specific speed curve options, the motor will never turn off, if speed is set to run at a minimum value with 0% duty cycle applied. In this type of configuration, standby mode is not available.



FG.
Open drain output, represents the speed of the motor for normal operation. Additionally, the FG pin serves as the data line, (SDA) for I2C communication.

RD.
Open drain output, Logic high indicates a rotor fault condition as defined by EEPROM variables. RD function can be disabled via EEPROM. When function is disabled RD pin goes high to indicate end of open loop starting sequence.

SPD.
Speed demand input. The demand can be in the form of duty cycle or analog voltage depending on the EEPROM setting. Additionally, the SPD pin serves as the clock line (SCL) for I2C communication.

CTAP.
This analog input is an optional connection for motor common (Wye motors). It is required to insert 2K ohm resistor in series with the pin. If not used, as in case of Delta wound motor, then pin must be left open circuit.

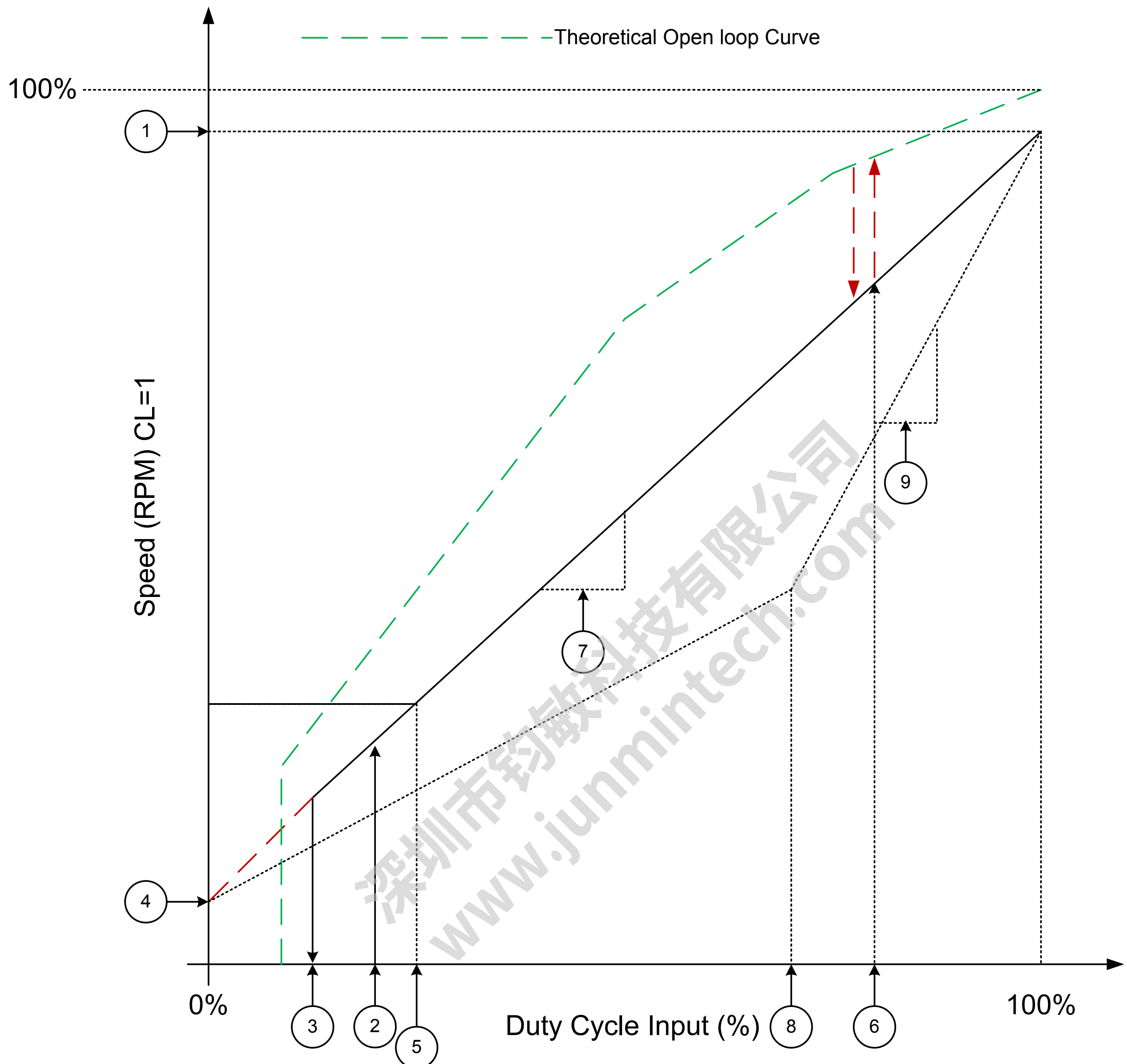
LOCK DETECT.
A5931 will turn off for the programmed time (t_{OFF}) when the rotor is in a locked condition.

OCP.
Overcurrent short protection will protect the IC from application conditions of motor output short to ground, shorted lead, or motor short to battery. The OCP protection monitors the drain to source voltage (VDS) across any source or sink driver when the output is turned on. The OCP level is approximately 5A. If the OCP threshold is exceeded for 640 nanoseconds, all drivers are shut off. This fault mode can be reset by PWM ON/OFF or timeout of t_{LOCK}, depending on EEPROM bit OCPOPT.

OCL.
An optional overcurrent limit function can be set to four different levels via EEPROM. In general the current limit should be set to a value beyond the maximum expected run current. If current limit occurs during normal operation, audible noise or motor stalling would potentially be observed. The current limit circuit monitors the VDS of the sink side MOSFET and turns off the source driver(s) for the remainder of the pwm cycle. Current Limit needs to be enabled via EEROM bit OCLD set low. If enabled, then OCL bits in the EEPROM control the level as follows.

Code	I_{OCL} (A)
00	3.2
01	2.4
10	1.6
11	.8

Speed Curve Parameters.



1. Maximum Speed (calculated from Slope of line AND Offset)
2. Duty On (DCON/511)
3. Duty Off (DCOFF/511
4. MINSPD
5. Min Duty Clamp
6. Max Duty Threshold and Hystersis
7. Slope (based on SPDSLP variable)
8. Slope Switch Duty
9. Slope 2 Option

Speed Curve Parameters (continued)
Refer to Figure 1 for below items.

Minimum Speed Set point.
The minimum speed is defined by the value stored in EEPROM variable MINSPD. The resolution is 1RPM.

MINSPD (RPM) = 0..4095

Maximum Speed Set point.
The A5931 calculates the maximum speed based on line equation y=mx + B. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable SPDSLP.

SPDSLP = 64*(Maximum Speed (Rpm) – MINSPD)/511

Example: Max Speed = 25000, Min Speed = 3000.

SPDSLP = 64*22000/511 = 2755

Where SPDSLP = 0..8192

Motor Speed (RPM) = Slope*DutyIN + MINSPD.

Where Slope = SPDSLP*511/64 and DutyIN expressed in %.

Duty In Enable Threshold.
EEPROM variable DCON defines the input duty signal that enables the drive. DCON is a 8 bit number with resolution of .2%, which results in a max setting of 49.9%.

Duty On (%) = 100*DCON/511

If DCON is set to "0", motor will turn on with 0% duty cycle input.

Duty In Disable Threshold.
EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8 bit number with resolution of .2%, which results in a max setting of 49.9%.

Duty Off(%) = DCOFF/511
DCOFF should always be set to a lower number than DCON.

Duty Cycle Invert.
To create mirror image of speed curve, set Duty cycle invert bit to "1".

Minimum Duty Clamp.
Minimum speed can be clamped to a value to allow motor to run at defined low level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

Min Duty Clamp (%) = 100*MINDTY/511

Therefore the minimum speed will be defined by:

MinSpeedClamp(RPM) = Slope*MinDutyClamp+MINSPD

Setting MINDTY to 0 disables the function.

MINDTY=0..255

Maximum Duty Clamp.
EEPROM variable DTYMAX defines a duty level at which the motor will change operation from closed loop curve. The change of operation would depend on MAXDTYOPT setting. If MAXDTYOP = 0, open loop operation will result, if MAXDTYOPT = 1 then operation will remain closed loop however the speed will be clamped at value calculated by DTYMAX level.

4 bits are used for this setting at resolution of 1.6% to cover the range 76.5% to 100%.

Maximum Duty (%) = 100*(511-MAXDTY*8)/511

MAXDTY = 0..15; If MAXDTY=0 then function is disabled.

Hysteresis is needed to prevent motor from going back and forth between open and closed loop mode.

MAXDTYHYS = 0...15

Hys(%) = (MAXDTYHYS+1)*.4

RD Function.

Rotor Lock output RD can be used to indicate motor is not running as expected. A high level on RD will indicate a fault.

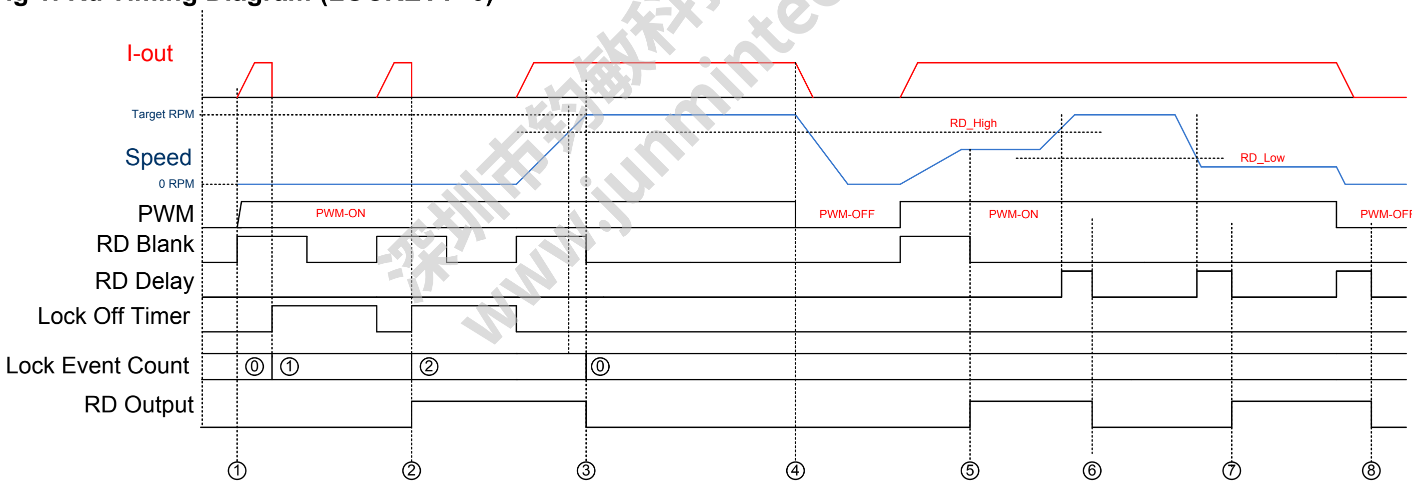
There are two situations for RD fault

1) Motor has lock events, enable into lock or lock while running.
    a. Rd signals after two consecutive lock events
    b. Lock Timer resets RD timer
2) Motor running and falls above and below defined thresholds
    a. Rd signals after RD Timer times out

There are two different methods for handling lock events, controlled by setting of EEPROM bit LOCKEVT.

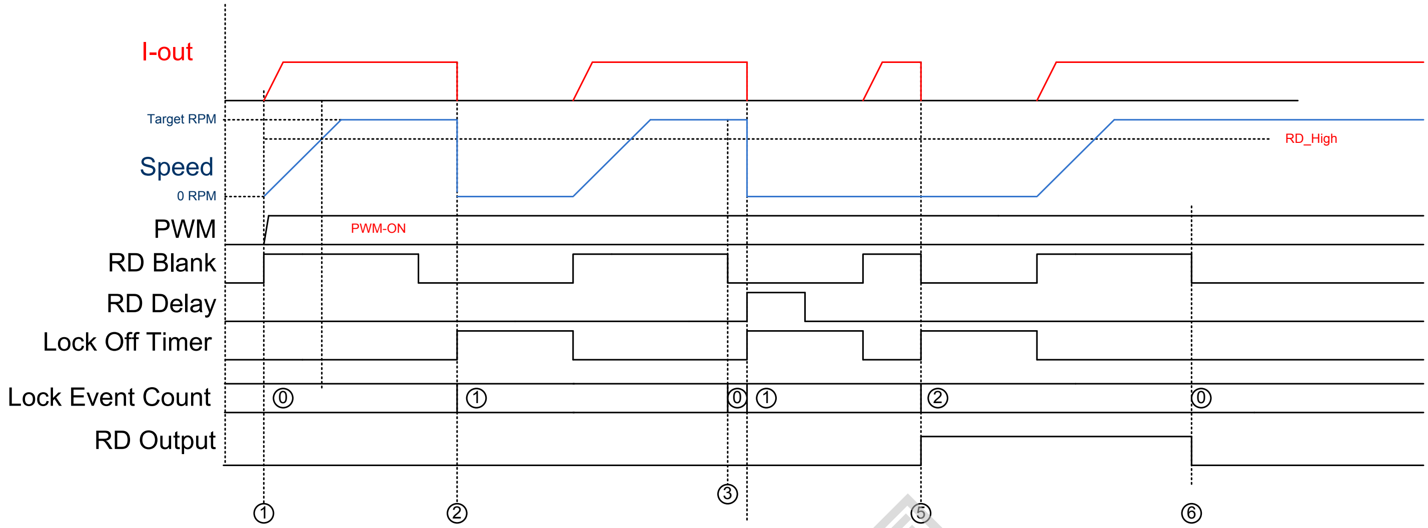
Parameter	Range	resolution	comment
LOCKEVT	0/1		0=RD triggered at lock event count of 2 1=Use RDBLANK for lock events
RD_High (RPM)	0 to 4080	16RPM	If set to 0; RD function disabled
RD_Low (RPM)	0 to 4080	16RPM	Must be programmed lower than RD_high
RDDLY	0 to 15	1S	
RDBLANK	.1 to 25.4	100ms	
T_LOCK_OFF	.1 to 25.4	100ms	

Fig 1: Rd Timing Diagram (LOCKEVT=0)



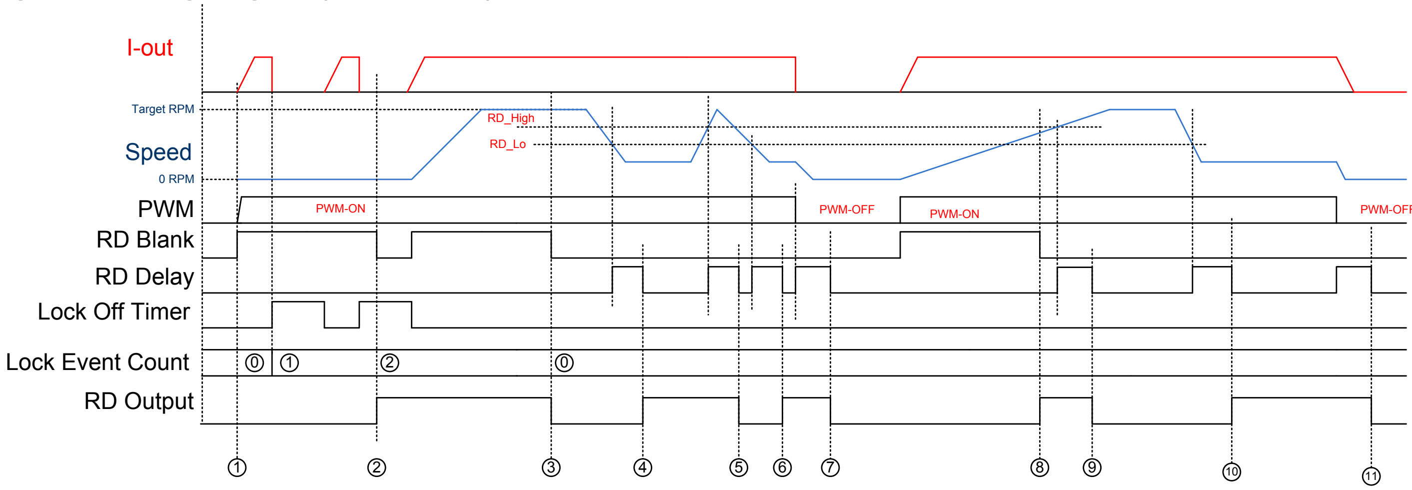
1. Power On with Rotor locked condition
2. Rd is High after 2nd lock event
3. Rd resets Low after RDBLANK if (Speed > RD_high); Lock Event count reset to Zero
4. PWM off – RD is low since normal condition
5. RD is High after RDBLANK if (Speed < RD_High)
6. Rd is Low if (Speed > RD_high) after RDDLY
7. Rd is High if (Speed < RD_Low) after RDDLY
8. PWM off – RD goes low after RDDLY low since normal condition

Figure 2 : Rd Timing Diagram (LOCKEVT=0) ; lock condition awhile running



1. Power On with PWM normal Startup
2. Rotor Locked while running – Lock Event counter is One
3. If Speed > RD_high after RDBLANK; Lock Event count reset to Zero
4. Rotor Locked while running – Lock Event counter is One
5. Rd is High after 2nd lock event
6. Rd reset to Low after RD BLANK if (Speed > RD_high); Lock Event count reset to Zero

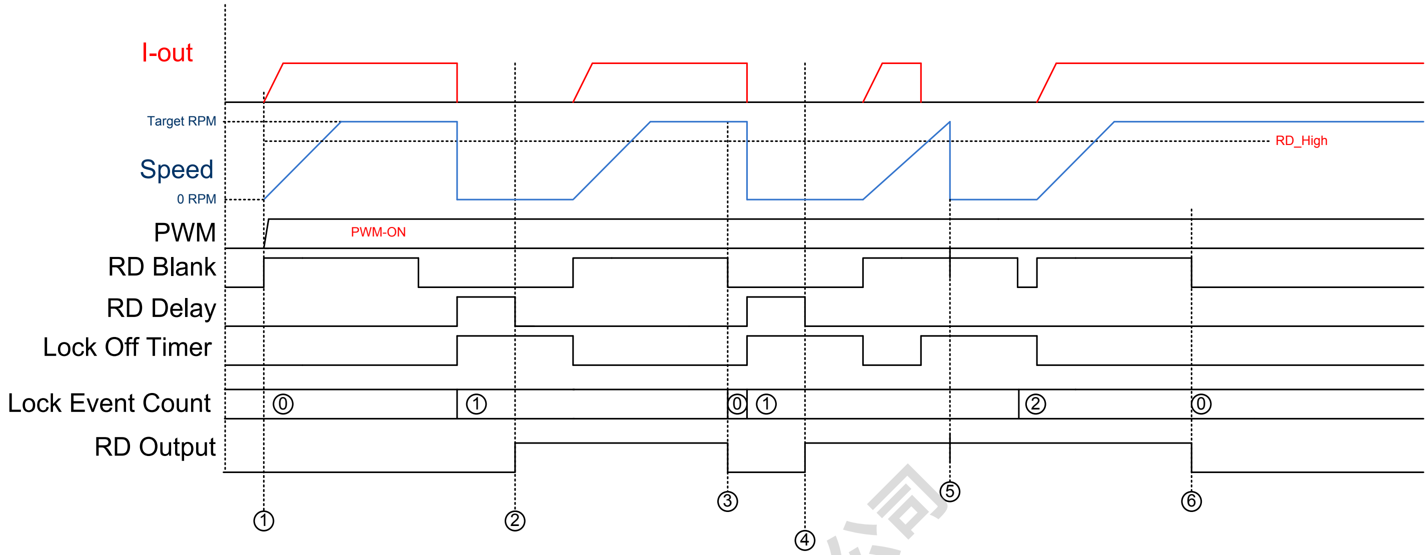
Fig 3: Rd Timing Diagram (LOCKEVT=1)



1. Power On with Rotor locked condition
2. Rd is High after RDBLANK if Speed < RD_High
3. Rd resets Low after RDBLANK if (Speed > RD_high)
4. RD changes to HI if speed < RD_low after RDDLY
5. RD changes to LO if speed > RD_high after RDDLY
6. RD changes to HI if speed < Rd_low after RDDLY
7. RD changes to LO when PWM goes off after RDDLY
8. RD changes to HI after RDBLANK is Speed < RD_high (even if > RD_low)
9. RD changes to LO if speed >R_high after RDDLY
10. RD changes to HI if speed < RD_low after RDDLY
11. RD changes to LO when PWM goes off after RDDLY

Note: RDBlank should be programmed longer than the time is take to accelerate to the RD_high level. Startup time + time to accelerate to RD_high.

Figure 4 : Rd Timing Diagram (LOCKEVT=1) lock condition while running



1. Power On with PWM normal Startup
2. Rotor Locked while running – RD changes to HI after RDDLY if Speed < RD_Low
3. RD changes to LO If Speed > RD_high after RDBLANK
4. Rotor Locked while running – RD changes to HI after RDDLY if Speed < RD_Low
5. Rd remains HI, even if speed is OK – since RDBLANK has not timed out.
6. Rd reset to Low after RD BLANK if (Speed > RD_high)

EEPROM MAP

ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
0	15:0	Dev1	Device Info for customer use	n/a	0
1	11:0	MINSPD	Range=0 to 4095, LSB=1RPM	2000	2000
	12	DUTYINV	0=Normal, 1=Invert	0	0
	13	MAXOFF	0=Normal, 1= Max speed when duty <DC_Off	0	0
	14	MAXDTYOPT	0=Run at Open Loop, 1=Run at MAXDTYCLP	1	1
	15	Unused			
2	13:0	SPDSLP1	Calculated Slope of Speed Curve	Set for 20000rpm	2254
	15:14	Unused		0	0
3	7:0	DCON	Range=0 to 49.9% LSB=.2%	10%	97
	15:8	DCOFF	Range=0 to 49.9% LSB=.2%	7.4%	79
4	3:0	MAXDTYCLP	Range= 100% to 76.5%, LSB=1.6%	0	0
	7:4	MAXDTYHYS	Range= 0 to 5.9%, LSB=.4%	0	0
	14:8	MINDTYCLP	Range= Range=0 to 49.9% LSB=.39%	0	0
	15	Unused			
5	7:0	STRTDMD	Range=0 to 16V, LSB=63mV	945mV	15
	15:8	DMDPOST	Range=0 to 100%, LSB=.39%	100%	255
6	7:0	ALIGNT	Range=0 to 20.4S LSB=80ms	480mS	6
	15:8	ASLOPE	Range= 160ms to 40S	511mS	80
7	7:0	STRTF	Range=0 to 20.4S LSB=80ms	2Hz	32
	15:8	ACCEL	Range= 0 to 99.6 Hz/S LSB=.78	42 Hz/S	107
8	7:0	ACCELT	Range=0 to 20.4S, LSB=80ms	480mS	6
	15:8	RMOT	Phase to Phase Motor Resistance (note1)	1.3	13
9	3:0	DMDRMPAL	Range=3.8 to 63.8ms/count, LSB=3.8	23.8ms/count	5
	7:4	DMDRMPAL	Range=3.8 to 63.8ms/count, LSB=3.8	7.8 ms/count	1
	11:8	DMDRMPDL	Range=3.8 to 63.8ms/count, LSB=3.8	15.8 ms/count	3
	15:12	DMDRMPDL	Range=3.8 to 63.8ms/count, LSB=3.8	15.8 ms/count	3
10	15:0	Dev2	Device Info for customer use	n/a	9
11	7:0	MAXSPD	Maximum Electrical Frequency	1061Hz	23
	15:8	TLOCK	0 to 25.5S	5S	50
12	7:0	RDLOW	Range=0 to 4095, LSB=16RPM	0	0
	15:8	RDHIGH	Range=0 to 4095, LSB=16RPM	0	0
13	7:0	RDBLK	Range=0 to 25.5S, LSB=100ms	0	0
	12:8	RDDLY	Range=0 to 15S, LSB=1S	0	0
14	11:0	PHASLP	Calculated Slope for Linear Phase Advance	Set for 11°@20000rpm	367
	15:12	SOWLIN	Window Width With Linear Phase Advance	28°	15

Note 1: R_{MOT} is for GUI use, it does not change operation of the IC

EEPROM MAP (Continued)

ADDR	Bits	Name	Description	Default Setting	Default Value (decimal)
15	0	PCDLY	Post Coast delay 0=100ms 1=500ms	500ms	1
	1	STBYDIS	Standby Mode 0=Enable 1=Disable	0	0
	3:2	PWMF	Motor PWM Selection	24/48kHz	2
	6	TCDIS	Temperature Compensation 0: ON 1:Off	0	0
	8:7	WINDM	Windmill Option	0	0
	12:9	SPDCLP	Minimum clamp is speed control mode	4.6%	2
	14:13	OCL	Set Overcurrent limit level	0	0
	15	OCLD	1=Disable Overcurrent LImit	0	0
16	0	CL	Speed Control Mode 0=OpenLoop 1=Closed	Enabled	1
	1	PHA	Running Mode 0=Auto 1=Linear Phase Advance	0	0
	2	RDOPT	Rd Function Mode select	0	0
	3	SPDSEL	Speed Control Select 0=PWM Duty, 1=Analog	0	0
	6:4	PP	Pole Pair = PP+1	2pp→4 pole motor	1
	7	NOCOAST	0=Coast After Start up Sequence 1= Do Not Coast	No – coast	1
	8	ALIGNMODE	0=Align 1=One Cycle	One cycle	1
	10:9	QCKSTRT	0=Disable 1= Enable	0	0
	11	FGSTRT	0=FG disabled during Startup, 1=FG Enabled	0	0
	13:12	BEMFHYS	Bemf Hys Level for Startup	40mV	1
	14	SOWAUTO	Initial Value of Window	21°	1
	15	OCPOPT	0=Reset after Tlock 1= After PWM on/off	T_{LOCK}	0
17	7:0	KP	Closed Loop	16	16
	15:8	KI	Closed Loop	2	2
18	7:0	SLPSWDTY	Duty at which slope changes	0	0
	15:8	Unused			
19	14:0	SLPSWRPM	Range 0 to 16384, LSB=1Rpm	2000rpm	2000
		Unused			
20	13:0	SPDSLP2	Calculated Slope	0	0
	15:14	Unused			
21	15:0	Allegro	Allegro Only Use	n/a	
22	15:0	Dev3	Device Info	n/a	
23	15:0	Allegro	Allegro Only Use	n/a	

Serial Port.
The A5931 uses standard fast mode I2C serial port format to program the EEPROM or to control the IC speed serially. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running the FG may pull then data line low while trying to initialize into serial port mode. Once a I2C command is sent the SPD input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The 5931 7 bit slave address is 0xXX).

I^{2}C Timing Diagrams.

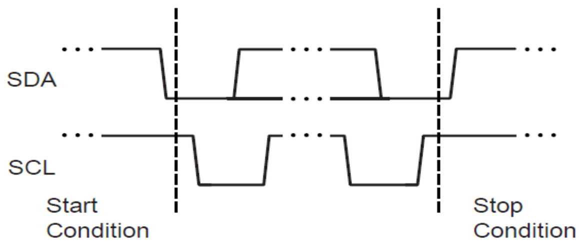


Figure 5. Start and Stop conditions

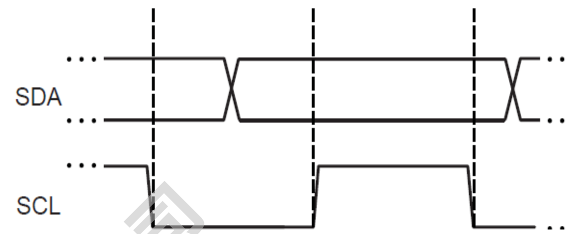


Figure 6: Clock and data bit synchronization

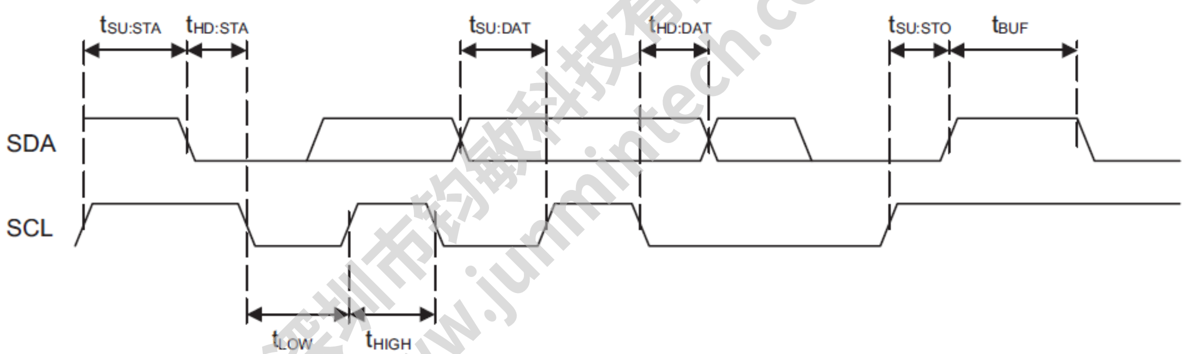


Figure 7: I2C™-Compatible Timing Requirements

Write command:

1) Start Condition
2) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3) Internal Register Address
4) 2 data bytes, MSB first
5) Stop Condition

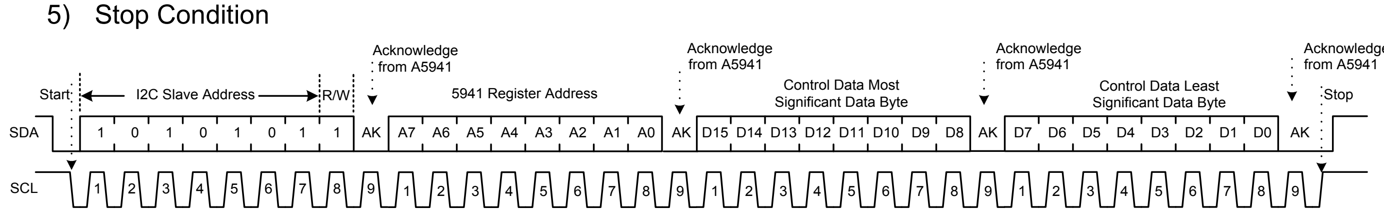


Figure 8: Write Command

Read command: Two Step Process

1) Start Condition
2) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 0
3) Internal Register Address to be read
4) Stop Condition
5) Start Condition
6) 7 bit I2C Slave Address (Device ID) 1010101, R/W Bit = 1
7) Read 2 data bytes
8) Stop Condition

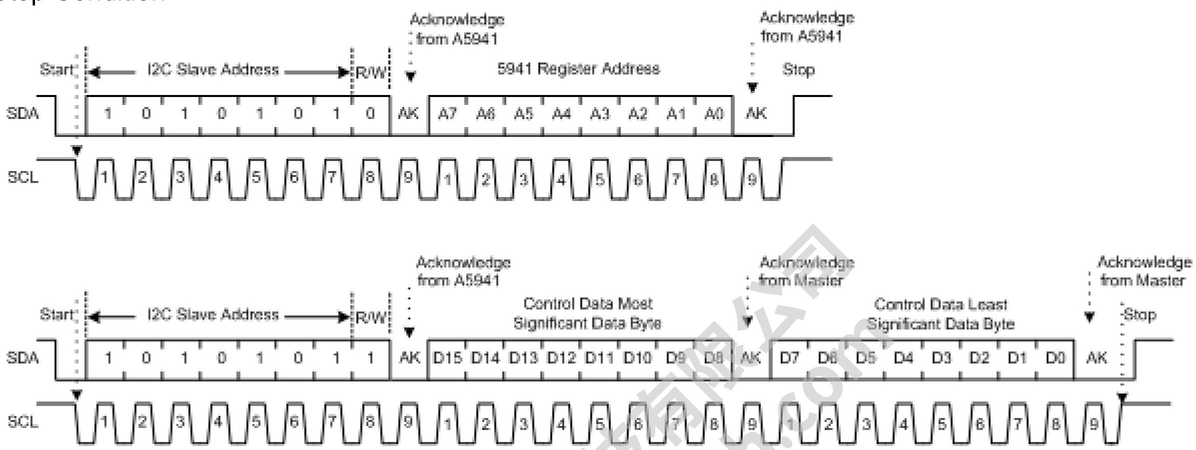


Figure 9: Read Command

Programming EEPROM. The A5931 contains 24words of 16 bit length. The EEPROM is controlled with the following i2c registers. Refer to application note for EEPROM definition.

EEPROM Control – Register **161**: Used to control programming of EEPROM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEProm Voltage required for Writing or Erasing
1	ER	Sets Mode to Erase
2	WR	Sets Mode to Write
3	RD	Sets Mode to Read
15:4	n/a	Do not use, always set to Zero during programming process

EEPROM Address– Register **162**: Used to set the EEPROM address to be altered

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory controlled
15:5	n/a	Do not use always set to Zero during programming process

EEPROM DataIn – Register **163**: Used to set the EEPROM new data to be programmed

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed.

EEPROM DataOUT – Register 164: Used for read operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

There are 3 basic commands, Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 10ms per word.
Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (hex=0x0105)

1) Erase the word

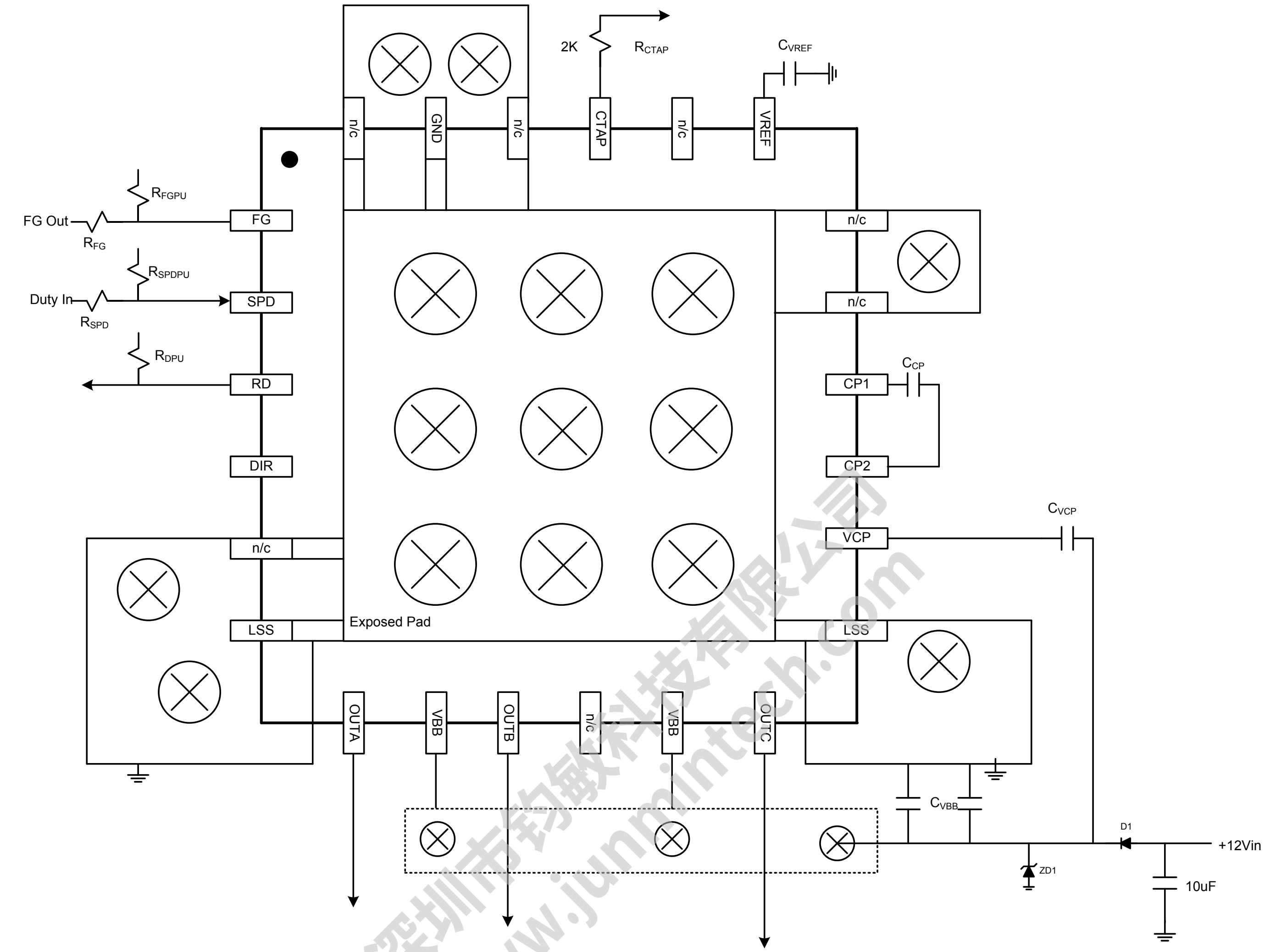
   I2c Write REGADDR[Data] ; comment
   a. 162[5] ; set EEPROM address to erase
   b. 163[0] ; set 0000 as Data In
   c. 161[3] ; set control to Erase and Voltage High
   d. Wait 10ms ; requires 10ms High Voltage Pulse to Write
   e. 161[0] ; clear Voltage
2) Write the new data
   a. 162[5] ; set EEPROM address to write
   b. 163[261] ; set Data In = 261
   c. 161[5] ; set control to Write and Set Voltage High
   d. Wait 10ms ; requires 10ms High Voltage Pulse to Write
   e. 161[5] ; clear Voltage

Example #2 Read address 5 to confirm correct data properly programmed.

1) Read the word

   I2c REGADDR[Data] ; comment
   a. 162[5] ; set EEPROM address to read
   b. 161[8] ; set control to Read
   c. 164[i2c read] ; readback from eeDataout
   d. 161[0] ; clear eeRead Bit

Layout.

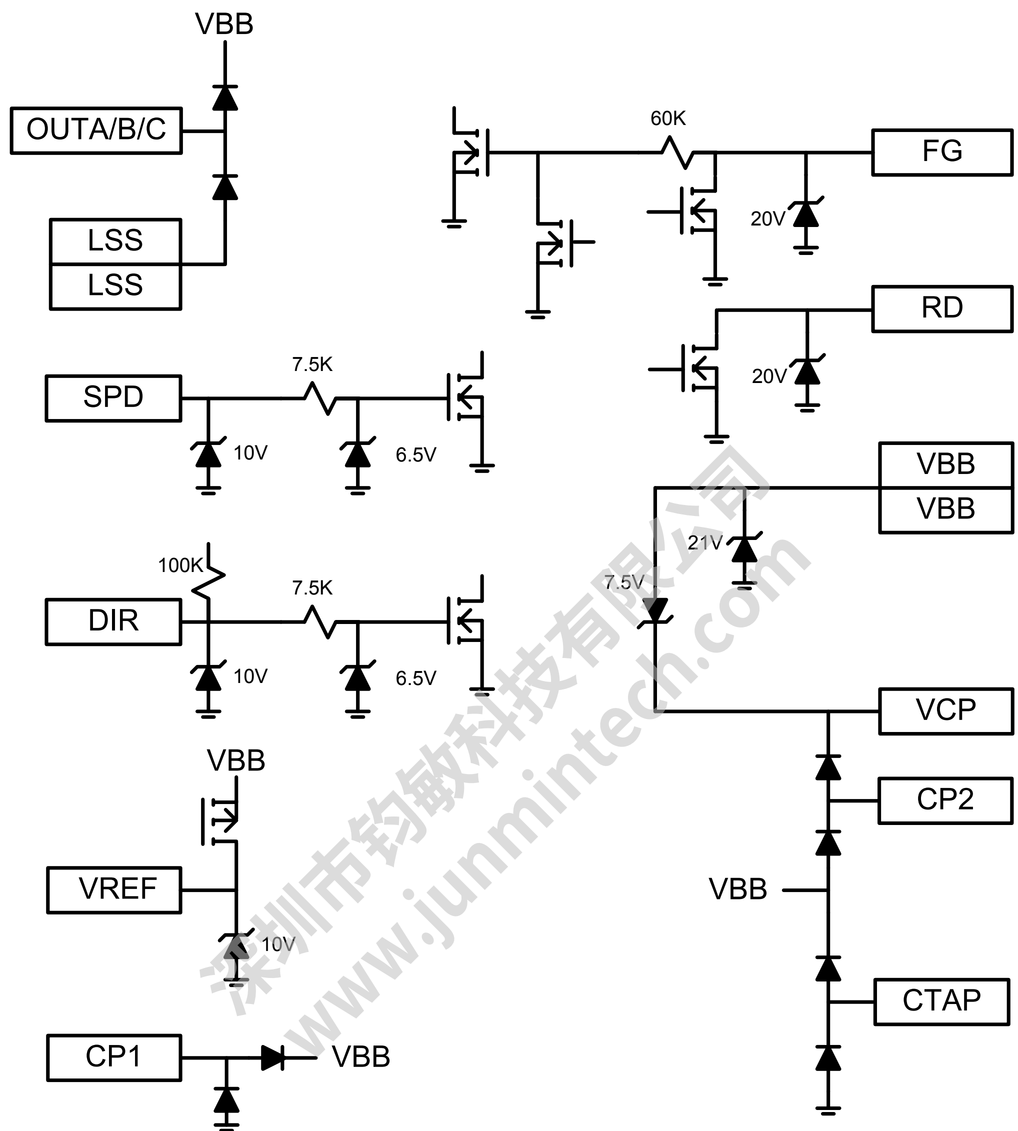


Name	Suggested	Comment
C_{VREF}	.1uF/X5R/10V	Ceramic capacitor required
CVBB	10uF-100uF	Power Supply Stabilization – Electrolytic or ceramic OK.
R_{FG}	10K	Pull up resistor for speed feedback
C_{VCP}	.1uF	Ceramic capacitor required
C_{CP}	.1uF	Ceramic capacitor required
D1	Not installed	May be Required to isolate motor from system or for reverse polarity protection
ZD1	SMBJ14A	TVS to limit max VBB due to transients due to motor generation or power line. Suggested to clamp below 18V.
R_{CTAP}	2K	2K series resistance ; Not required if pin left O/C
R_{FG}	500	Optional – If FG wired to connector – R_{FG} will isolate IC pin from noise or overvoltage transients or protect from connector issues
R_{FGPU}	10K	Open Drain Pull Up resistor – Required if using pin for i2c
R_{SPD}	500	Optional – If PWM wired to connector – R_{SPD} will isolate IC pin from noise or overvoltage transients or protect from connector issues
R_{SPDPU}	10K	Open Drain Pull Up resistor – Required if using pin for i2c
R_{RD}	10K	Open Drain Pull Up resistor - Optional fro RD function or test use.

Layout Notes.

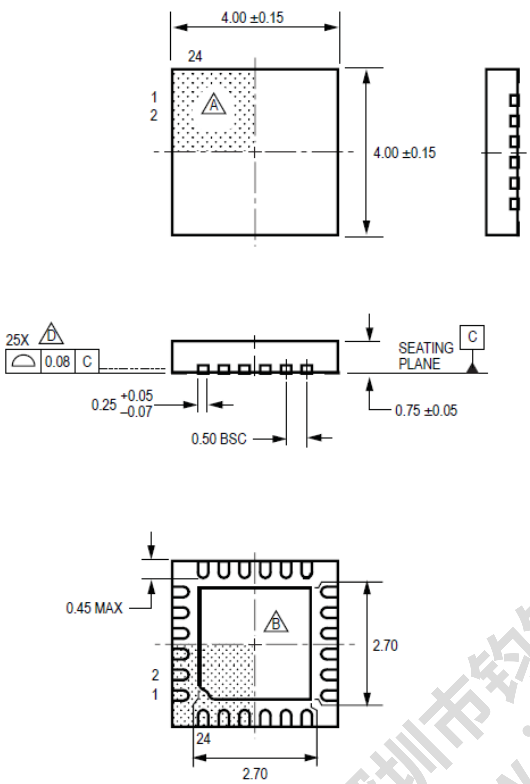
1) Add thermal vias to exposed pad area.
2) Add ground plane on top and bottom of PCB.
3) Place CVREF & CVBB as close as possible to IC, connected to GND plane

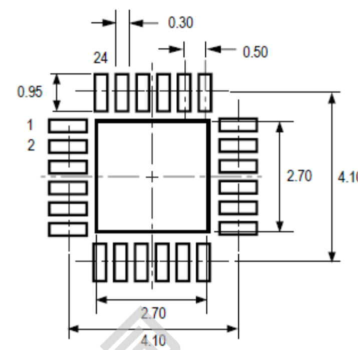
Pin Diagrams



Package Drawing

ES Package, 24-Pin QFN with Exposed Thermal Pad





C PCB Layout Reference View

For Reference Only; not for tooling use (reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package LP, 16-Pin TSSOP with Exposed Thermal Pad