A5941

Three Phase Sensorless Fan Driver

FEATURES AND BENEFITS

- Quiet Startup
- 180 Degree Sinusoidal Drive For Low Audible Noise
- High Efficiency Control Algorithm
- Sensorless Operation
- Wide supply voltage range
- FG Speed Output
- Lock Detection
- Overcurrent Protection
- Soft Start
- Short Circuit Protection

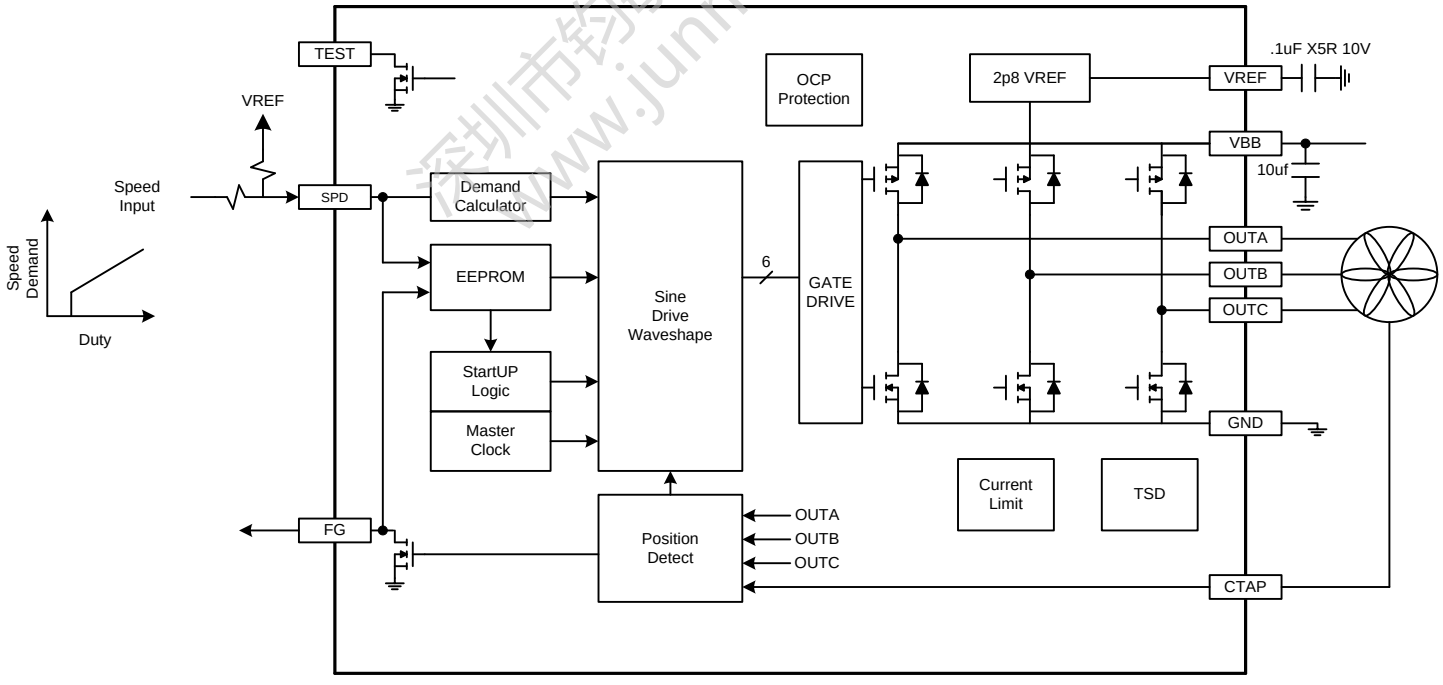
DESCRIPTION

The A5941 three phase motor drivers incorporate sinusoidal drive to minimize audible noise and vibration for medium power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly startup and gradually ramp up the motor to desired speed. The voltage profile is set to a default value that will operate for a wide range of motor characteristics. EEPROM can be altered to customize the startup operation if desired.

The motor speed is controlled by applying a Duty cycle command to the PWM input The PWM input is allowed to operate over a wide frequency range. If desired and analog voltage can be used to control motor speed, set via EEPROM adjustment.

The A5941 is available in a 10L SOIC (suffix LN), and a 10 lead SOIC with exposed pad (suffix LK).



Typical Application

Selection Guide

Part Number	Ambient Temp Range	Package	Packing
A5941GLKTR-T	-40 to 105C	10L SOIC with Exposed Pad	3000 pieces per 13 in reel
A5941GLNTR-T	-40 to 105C	10L SOIC	3000 pieces per 13 in reel

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}				18	V
Input Voltage Range	V_{IN}	SPD	-.3		5.5	V
Logic Output	Vo	FG			18	V
Logic Output Current	Io	FG			10	mA
Output Current	I_{OUT}	Internally Limited			I_{OCLMAX}	A
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta	Range G	-40		105	°C
Package Thermal Resistance						
LK Package	Rja	2 sided PCB 1 in^2 Copper		45		°C/W
LN Package		Single sided PCB		130		

TERMINAL LIST

Pin Name	Pin Description	Num
SPD	Speed Input	1
FG	Speed Output Signal	2
VBB	Input Supply	3
OUTA	Motor Terminal	4
OUTB	Motor Terminal	5
GND	Ground	6
OUTC	Motor Terminal	7
VREF	Analog Output	8
TEST	Logic Output	9
CTAP	Analog Input	10

ELECTRICAL CHARACTERISTICS, G version : Valid at T_A = +25°C, VBB = 4V to 18V

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	I_{BB}			7	9	mA
Total Driver Rdson (Sink + Source)	R_{DSON}	I = 1A, Tj=25C, VBB=12V	1	1.25	1.5	Ohm
		I = 1A, Tj=25C, VBB=4V		1.9		Ohm
		Source Driver		870	1150	mΩ
		Sink Driver		380	450	mΩ
VREF	V_{REF}	I_{OUT}=5mA		2.8		V
Input Current (SPD)	Iin	Vin=0 to 5.5V	-5	<1	5	uA
Logic Input Low Level	V_{IL}		0		.8	V
Logic Input High Level	V_{IH}		2		5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Sat Voltage	V_{SAT}	I=5mA			.3	V
FG Output Leakage	I_{FG}	V=18V, Motor Drive Disabled			1	uA
SPD Input (vsp mode)						
SPD On Threshold	VTH_{ON}		210	250	290	mV
SPD Off Threshold	VTH_{OFF}		160	200	240	mV
SPD MAX	VTH_{MAX}			2.5		V
Resolution				4.89		mV
Accuracy				+/- 6LSB		
SPD Input (pwm mode)						
PWM On Threshold	DC_{ON}			10		%
PWM Off Threshold	DC_{OFF}			7.5		%
PWM Input Frequency Range	F_{PWM}		2.5		100	Khz
Motor PWM Frequency	Fpwm		23.2	24.4	25.6	kHz
VBB UVLO	VBB_{UVLO}	VBB rising		3.85	3.98	V
VBB UVLO HYS	VBB_{HYS}		150	300	450	mV
Lock Protection	t_{OFF}	Relative to Target		+/-7		%
Overcurrent	I_{OCL}		1.4	1.6	1.8	A
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing.	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		20		°C

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

Functional Description

The A5941 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds. The trapezoidal startup method does not require any external components and will automatically switch to sinusoidal operation as the motor is accelerating up to operating speed.

The speed of the fan can be controlled by voltage mode (control of power supply amplitude), variable duty cycle PWM input or via an adjustable analog input. Use of the PWM or analog input allows overall system cost savings by eliminating the requirement of an external variable power supply. Operation down to 4V can be achieved to allow the IC to fit into legacy systems with voltage mode operation.

The SPD input (duty or analog voltage) is measured and converted to a 9bit number. This 9 bit "demand" is applied to a pwm generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A bemf detection "window" is opened on phase A modulation profile in order to measure the rotor position so as to define the modulation timing. The control system maintains the window to a small level in order to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor and thermal shutdown.

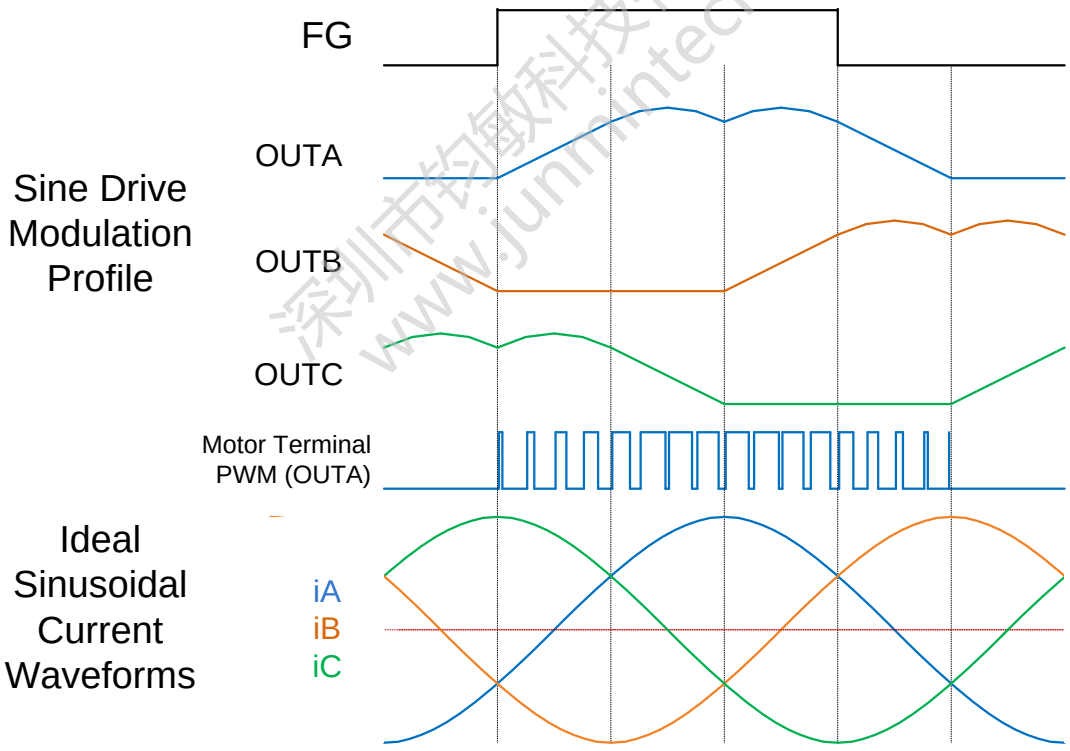


Figure 1: Sinusoidal PWM

Speed Control.

Duty Cycle Input. A duty cycle measurement circuit converts the applied duty to a demand value (9 bit resolution) to control speed of the fan. The motor drive will be enabled if duty is larger than DC_ON. The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

Power Supply Modulation. Speed can be controlled simply by varying the power supply voltage. Motor Drive will be enabled and disabled at undervoltage rising and falling thresholds.

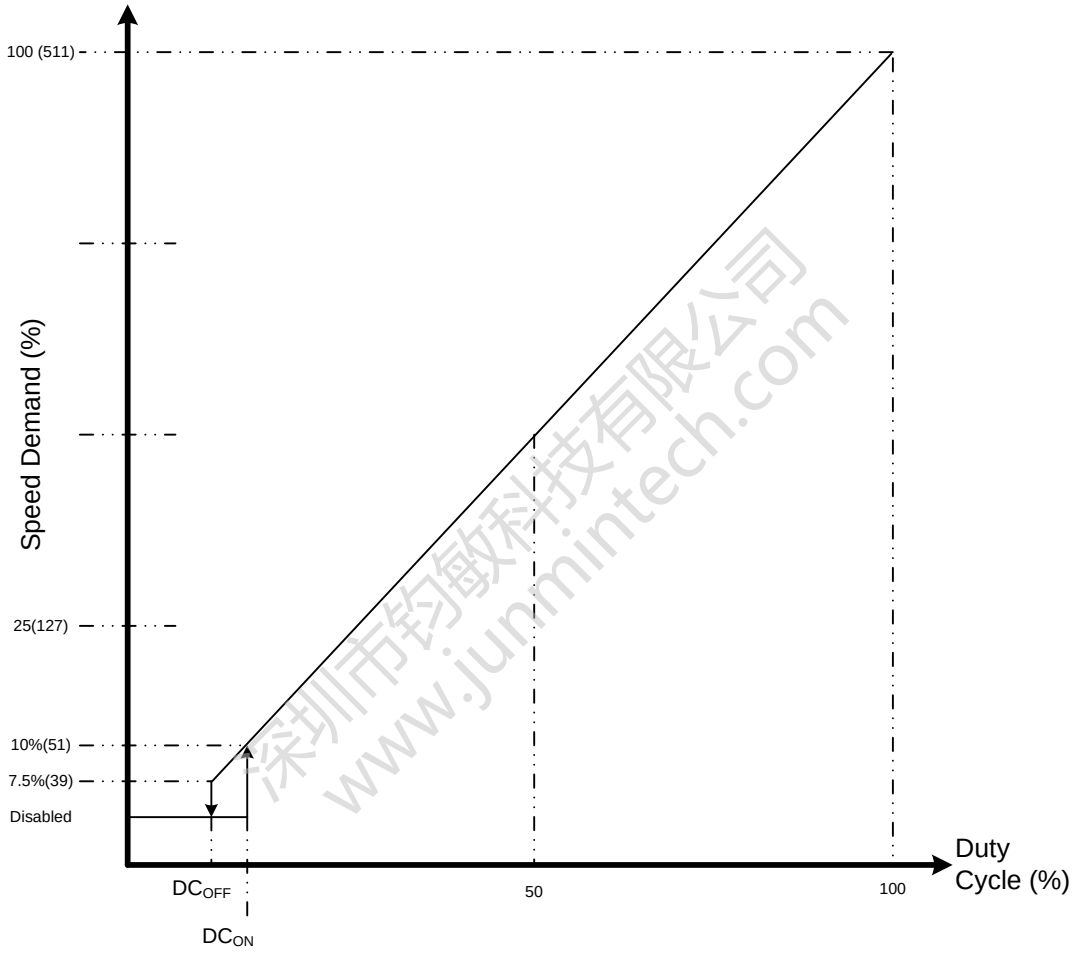


Figure 2) PWM Speed Input Characteristic

Analog Input. An internal ADC translates the input voltage to a demand value to control speed of the fan. The motor drive will be enabled if SPD is higher than VTH_{ON} and disabled if lower than than $VTH_{OFF.}$

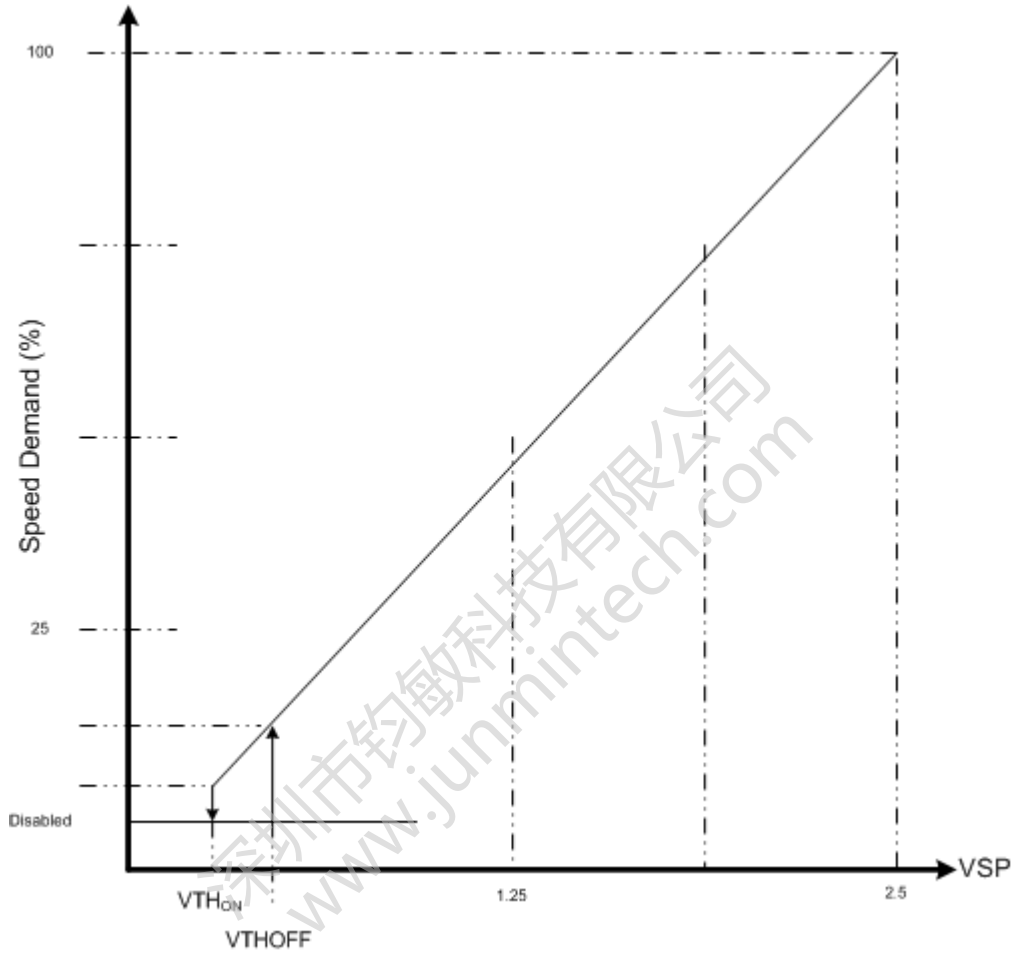


Figure 3) Analog Speed Input Characteristic

Note: Default Setting for A5941 is PWM duty input.

Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for T_{OFF} before an auto-restart is attempted.

FG. Open drain output provides speed information to the system. FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

CTAP. Connection terminal for motor common for Wye connected motors. A virtual centertap is created internally if motor common is not available or Delta type motor is used. The CTAP pin should be left open if not used.

Current Limit. Load Current is monitored on the low side MOSFET. If the current has reached $I_{OCL,}$ the source drivers will turn off for the remaining time of the PWM cycle.

TEST. Logic output provides signals for production test of IC. Pin should be left open or pulled up to VREF with 10K resistor in application circuit.

Quiet Startup.

A5941 controls startup in three stages as represented in below figure:

1) Align/Hold – Moves motor to known starting position
2) Ramp up motor speed – Accelerate with modulation profile applied to motor windings in Open Loop (no position measurement)
3) Ramp to final value of External Duty (or 100% for Power Supply Speed control system). This occurs after switching to position sensing mode.

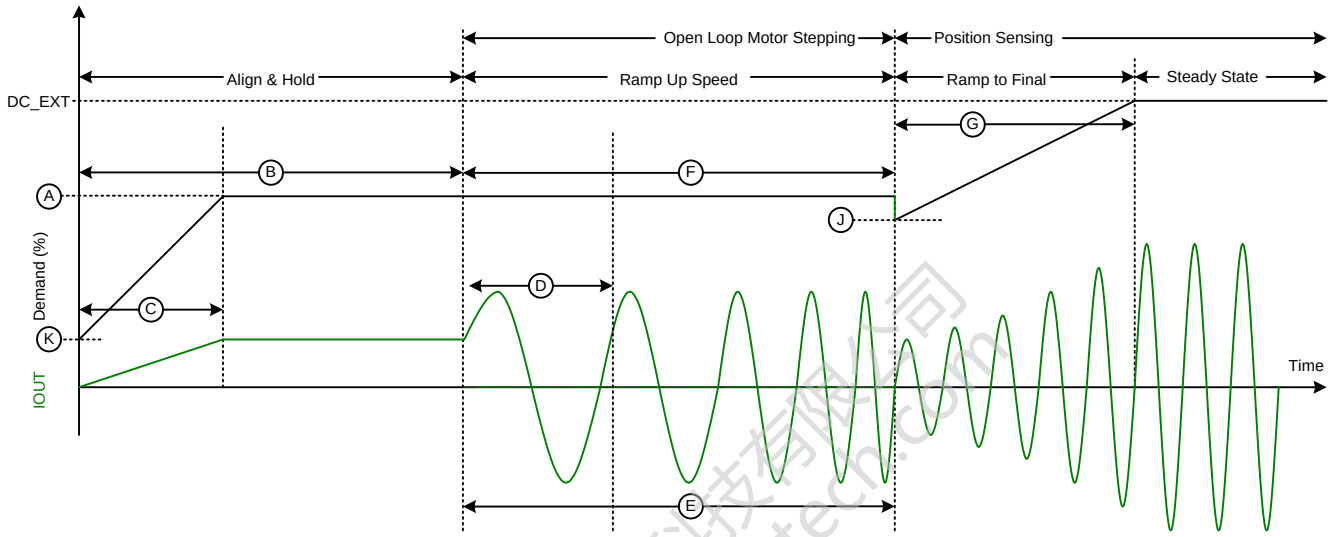
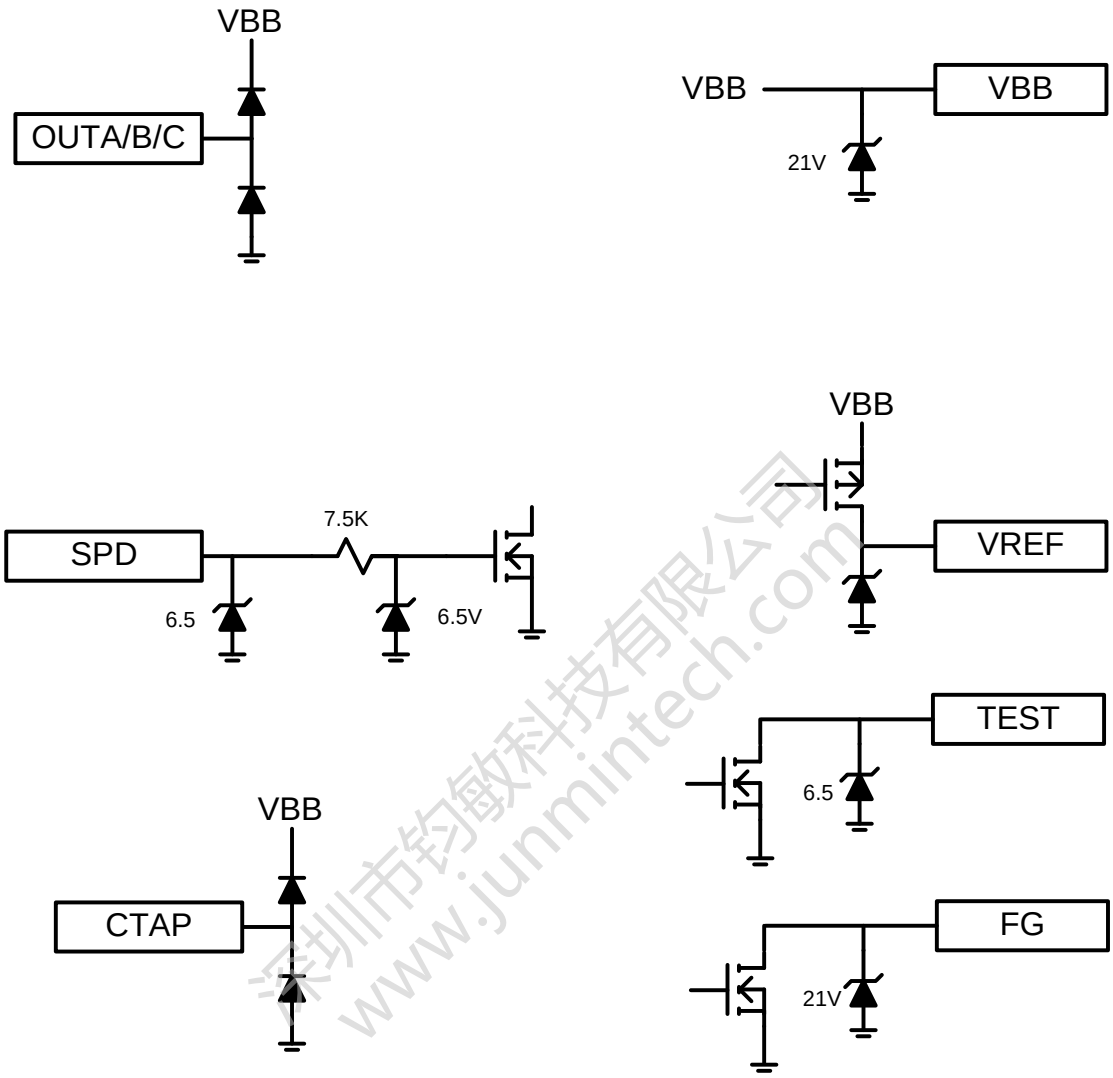


Fig 1. Applied Demand (Modulated voltage) and Resultant Iout Typ. Wave during Startup

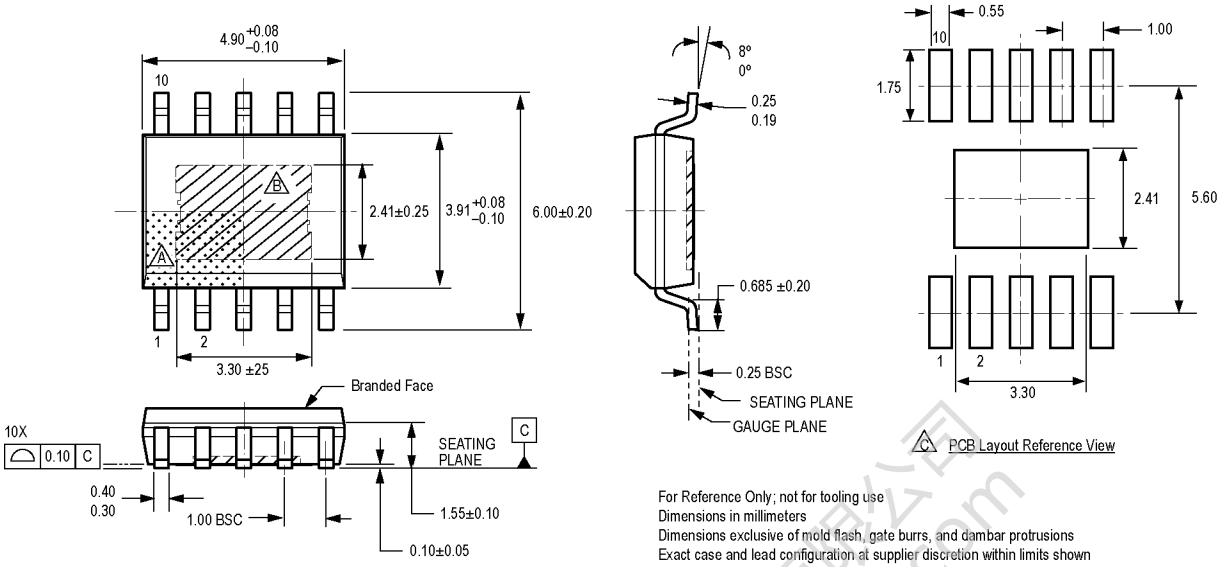
	Variable	Setting	Description
(A)	STRTDMD	25%	Demand level During Open Loop Startup
(B)	ALIGNT	2S	Total Duration of Alignment phase
(C)	ALIGNRMP	40%/Sec	Demand Ramp Rate during alignment
(D)	STRTF	.25 Hz	Starting Frequency
(E)	ACCEL	4 Hz/S	Acceleration Rate
(F)	ACCELT	1.8S	Total Duration of Acceleration Phase
(G)	DMDRMP	15%/Sec	Demand Ramp Rate
(J)	DMDPOST	20%	Initial Demand starting point after OPEN loop mode
(K)	ALIGNINI	6%	Initial Align Demand level

Note: Duty cycle demand levels stated above (A, J, K) are for VBB=12V. For lower power supply voltages the demand level is compensated for by approximately 5% per Volt.

Pin Diagrams



Package LK, 10-Pin Exposed pad SOIC



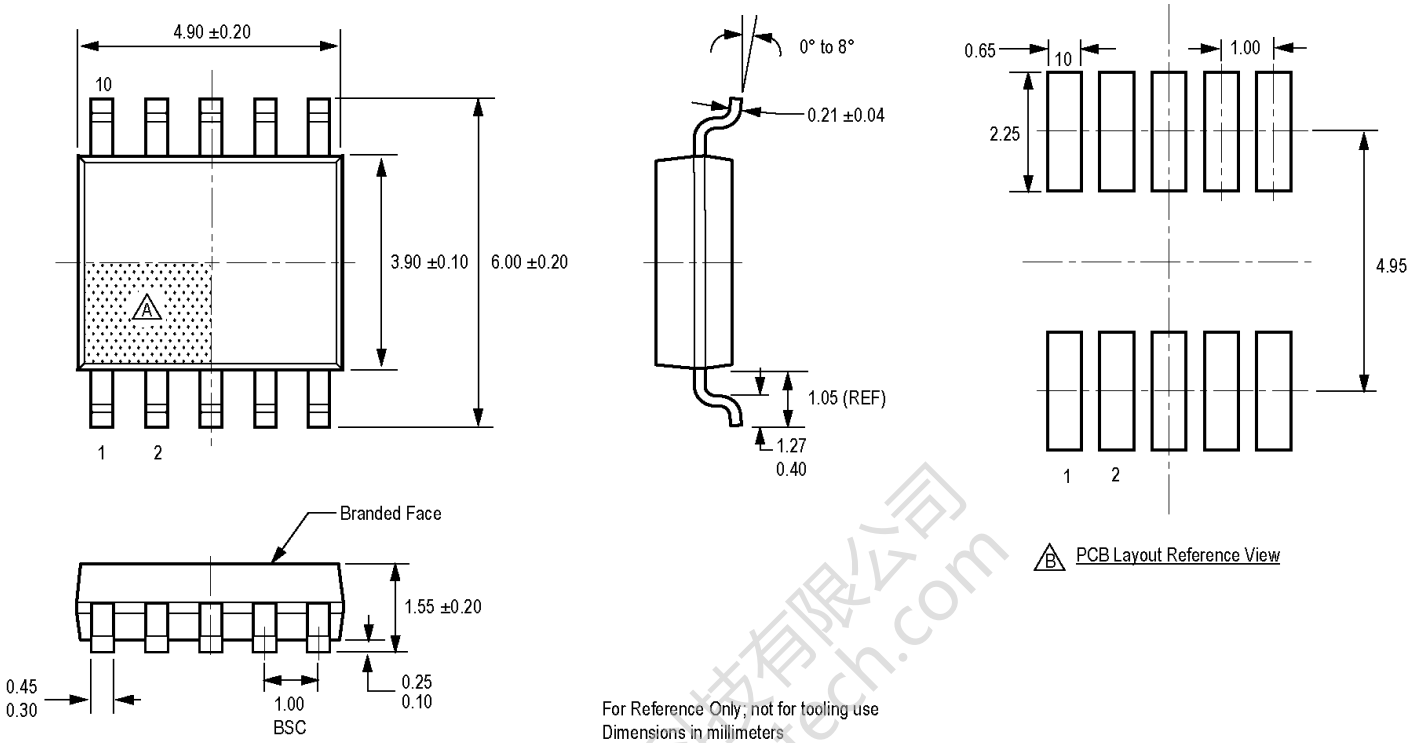
For Reference Only; not for tooling use
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LN, 10 pin SOIC



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A Terminal #1 mark area

B Reference land pattern layout. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias near the pin lands can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-7)