Single Phase Full-Wave Motor Driver for Fan Motor AM7228S

This is the summary of application for AM7228S optimum for driving 12V fan for general consumer equipment. The most attractive function of AM7228S is slope adjust by external resistor, that can meet most of fan request. This IC employs soft switching drive, Bi-CMOS process, and realizes silent drive, low ON resistor, and low power consumption. This also incorporate lock protection and auto restart circuit which does not require external capacitor.

Applications

Optimum for driving 12V fan for general consumer equipment

Features

1) Slope adjust mode for VH and VL pin control.
2) Soft switched drive.
3) PWM speed control.
4) Rotating speed pulse signal (FG) output.
5) Incorporating lock protection and automatic restart circuit.
6) Power Tr incorporated.
7) Hall Bias voltage built-in.
8) Soft start function built-in for reducing power up acoustic noise.
9) Stop mode duty adjustable.

Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	18	V
Output current	Iomax	1200	mA
FG single output current	I_{FG}	10	mA
FG single output voltage	V_{FG}	18	V
Vref output current	Iref	10	mA
HB output current	I_{HB}	10	mA
High duty slope setting voltage	VH	6	V
Low duty slope setting voltage	VL	6	V
Stop mode setting voltage	VStop	6	V
Power dissipation (JEDEC 2S2P PCB)	Pd	3030*	mW
Operate temperature range	T_{opr}	-40～+105	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	Tjmax	150	℃

* Pd de-rated by 24.2mW/°C over 25℃ (based on JEDEC 2S2P board)

Those are stress rating only and functional operating at those conditions for extended periods may damage to the device.

Recommended operating conditions

(Set the power supply voltage taking allowable dissipation into considering)

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage range	Vcc	2.5～16			V
Hall input voltage range	V_{HB}	0.2～2.1			V
High duty slope setting voltage range	VH	0~Vref			V
Low duty slope setting voltage range	VL	0~Vref			V
Stop Mode setting voltage range	VStop	0~Vref			V

Electrical Characteristics

(Unless otherwise specified, Ta = 25℃, VCC = 12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply current 1	$I_{CC}1$	1	3	6	mA	PWM=GND
Supply current 2	$I_{CC}2$	2	5	8	mA	PWM=OPEN
Reference Voltage	VREF	4.5	5	5.5	V	Ivref=5mA
Hysteresis of STOP mode	VStopH	50	110	170	mV	Vref=5V
Hall input						
Input offset voltage	V_{HOFS}	—	—	±6	mV	
PWM input						
Input H level	V_{PWMH}	2.5	—	Vref	V	
Input L level	V_{PWML}	-0.3	—	0.8	V	
Input frequency	F_{PWM}	5	—	100	kHz	
Output						
Output voltage	V_0	—	0.4	0.6	V	I_0=200mA(Upper + Lower)
Input-output Gain	G_{IO}	51	54	57	dB	
FG low voltage	V_{FGL}	—	0.3	0.4	V	I_{FG} = 5mA
FG leakage current	I_{FGL}	—	—	20.0	μA	V_{FG} = 15V
Input hysteresis voltage	V_{HYS}	±10	±17	±25	mV	
Hall bias voltage	V_{HB}	1.0	1.15	1.3	V	I_{HB}=-5mA
Lock protection						
Lock detection ON time	T_{ON}	0.35	0.50	0.65	Sec	
Lock detection OFF time	T_{OFF}	3.5	5.0	6.5	Sec	

Block Diagram

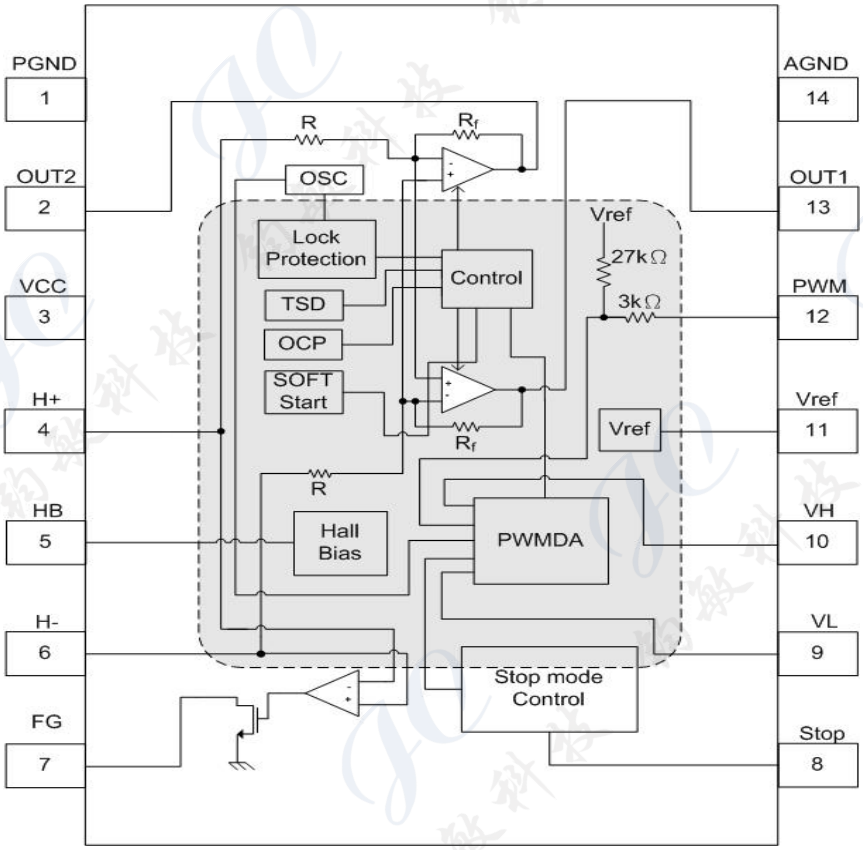


Fig1. Block diagram

Pin Description

PIN No	Pin Name	Function	PIN No	Pin Name	Function
1	PGND	Power ground terminal	8	Stop	Stop mode setting terminal
2	OUT2	Motor output terminal	9	VL	Low duty slope setting terminal
3	VCC	Power supply terminal	10	VH	Hi duty slope setting terminal
4	H+	Hall input terminal	11	VREF	Reference voltage output terminal
5	HB	Hall Bias	12	PWM	PWM signal input terminal
6	H-	Hall input terminal	13	OUT1	Motor output terminal
7	FG	FG signal output terminal	14	AGND	Analog ground terminal

Truth Table

H+	H-	PWM	OUT1	OUT2	FG	Mode
H	L	H	H	L	L (Output Tr : ON)	Operation mode
L	H		L	H	Z (Output Tr : OFF)	
H	L	L	L	L	L (Output Tr : ON)	
L	H		L	L	Z (Output Tr : OFF)	
H	L	-	L	L	L (Output Tr : ON)	Lock mode
L	H		L	L	Z (Output Tr : OFF)	

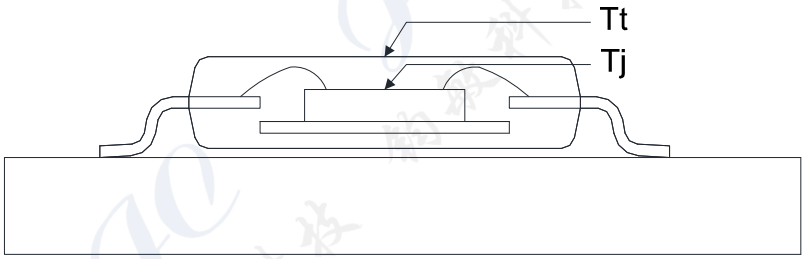
Z：Open drain output (High impedance)

Thermal Information

Θja	junction-to-ambient thermal resistance	41.25℃/W
Ψjt	junction-to-top characterization parameter	1.34℃/W

- **Θja** is obtained in a simulation on a JEDEC-standard 2s2p board as specified inJESD-51.
- The **Θja** number listed above gives an estimate of how much temperature rise is expected if the device was mounted on a standard JEDEC board.
- When mounted on the actual PCB, the **Θja** value of JEDEC board is totally different than the **Θja** value of actual PCB.
- **Ψjt** is extracted from the simulation data to obtain **Θja** using a procedure described in JESD-51, which estimates the junction temperature of a device in an actual PCB.

- The thermal characterization parameter, **Ψjt**, is proportional to the temperature difference between the top of the package and the junction temperature. Hence, it is useful value for an engineer verifying device temperature in an actual PCB environment as described in JEDEC JESD-51-12.
- When Greek letters are not available, **Ψjt** is written Psi-jt.
- Definition:



DFEINITION: $\psi_{jt} = (T_j - T_t) / P_d$

Where :

Ψjt (Psi-jt) = Junction-to-Top(of the package) °C/W
Tj= Die Junction Temp. °C
Tt= Top of package Temp at center. °C
Pd= Power dissipation. Watts

- Practically, most of the device heat goes into the PCB, there is a very low heat flow through top of the package, So the temperature difference between **Tj** and **Tt** shall be small, that is any error caused by PCB variation is small.

- This constant represents that **Ψjt** is completely PCB independent and could be used to predict the **Tj** in the environment of the actual PCB if **Tt** is measured properly.

- **How to predict Tj in the environment of the actual PCB**

Step 1 : Used the simulated **Ψjt** value listed above.

Step 2 : Measure **Tt** value by using

- **Thermocouple Method**
  We recommend use of a small ~40 gauge(3.15mil diameter) thermocouple. The bead and thermocouples wires should touch the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be heat-insulated to prevent cooling of the bead due to heat loss into wires. This is important towards preventing "too cool" **Tt** measurements, which would lead to the calculated **Tj** also being too cool.

- **IR Spot Method**
  An IR Spot method should be utilized only when using a tool with a small enough spot area to acquire the true top center "hot spot".
  Many so-called "small spot size" tools still have a measurement area of 0~100+mils at "zero" distance of the tool from the surface. This spot area is too big for many smaller packages and likely would result in cooler readings than the small thermocouple method. Consequently, to match between spot area and package surface size is important while measuring **Tt** with IR sport method.

Step 3 : calculating power dissipation by

$$P \cong (VCC - |Vo_{Hi} - Vo_{Lo}|) \times I_{out} + VCC \times Icc$$

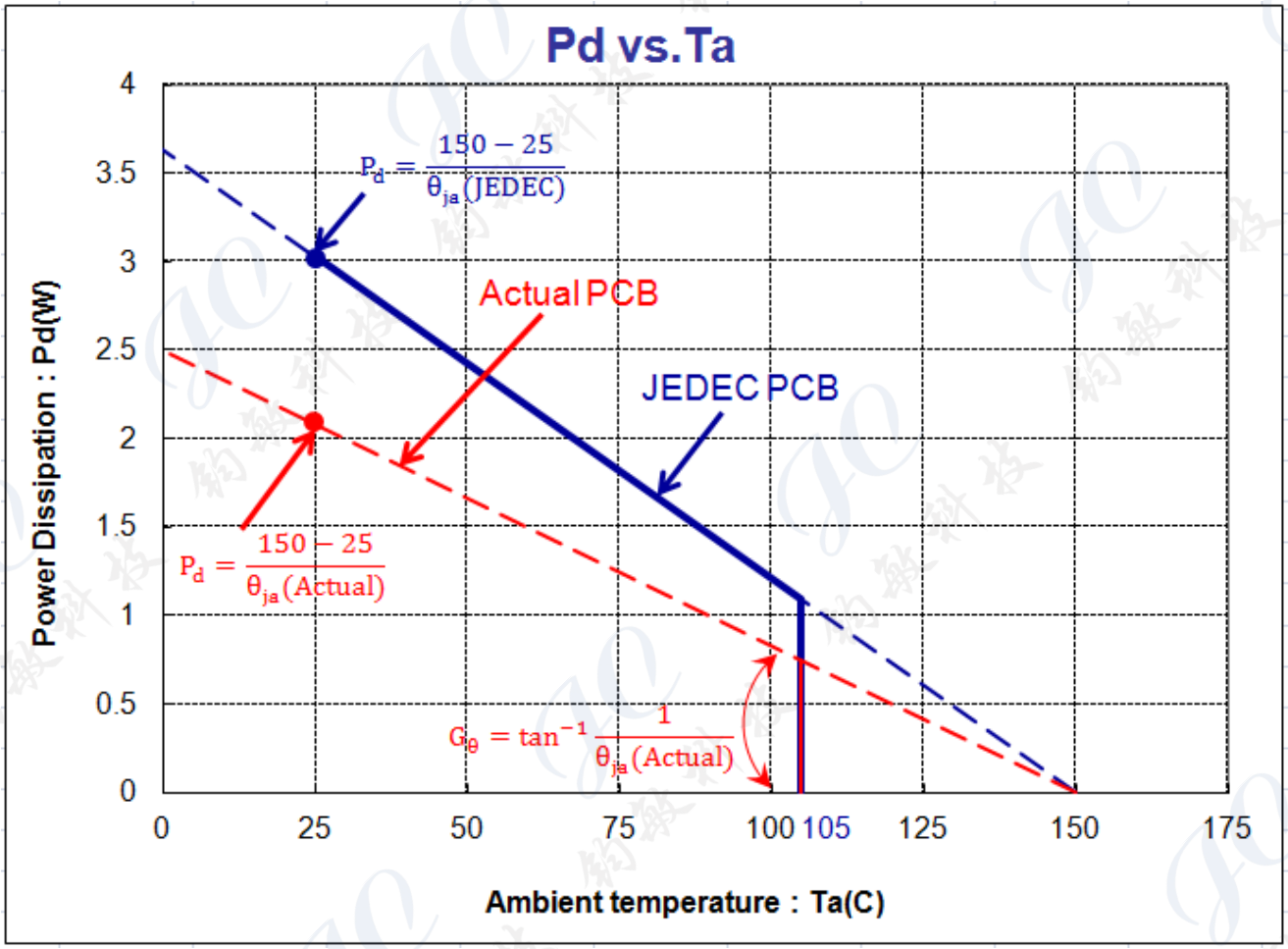
Step 4 : Estimate **Tj** value by

$$Tj = \Psi jt \times P + Tt$$

Step 5: Calculated Θja value of actual PCB by the known **Tj**

$$\Theta ja(actual) = (Tj - Ta)/P$$

Maximum Power Dissipation (de-rating curve) under JEDEC PCB & actual PCB



Application circuit

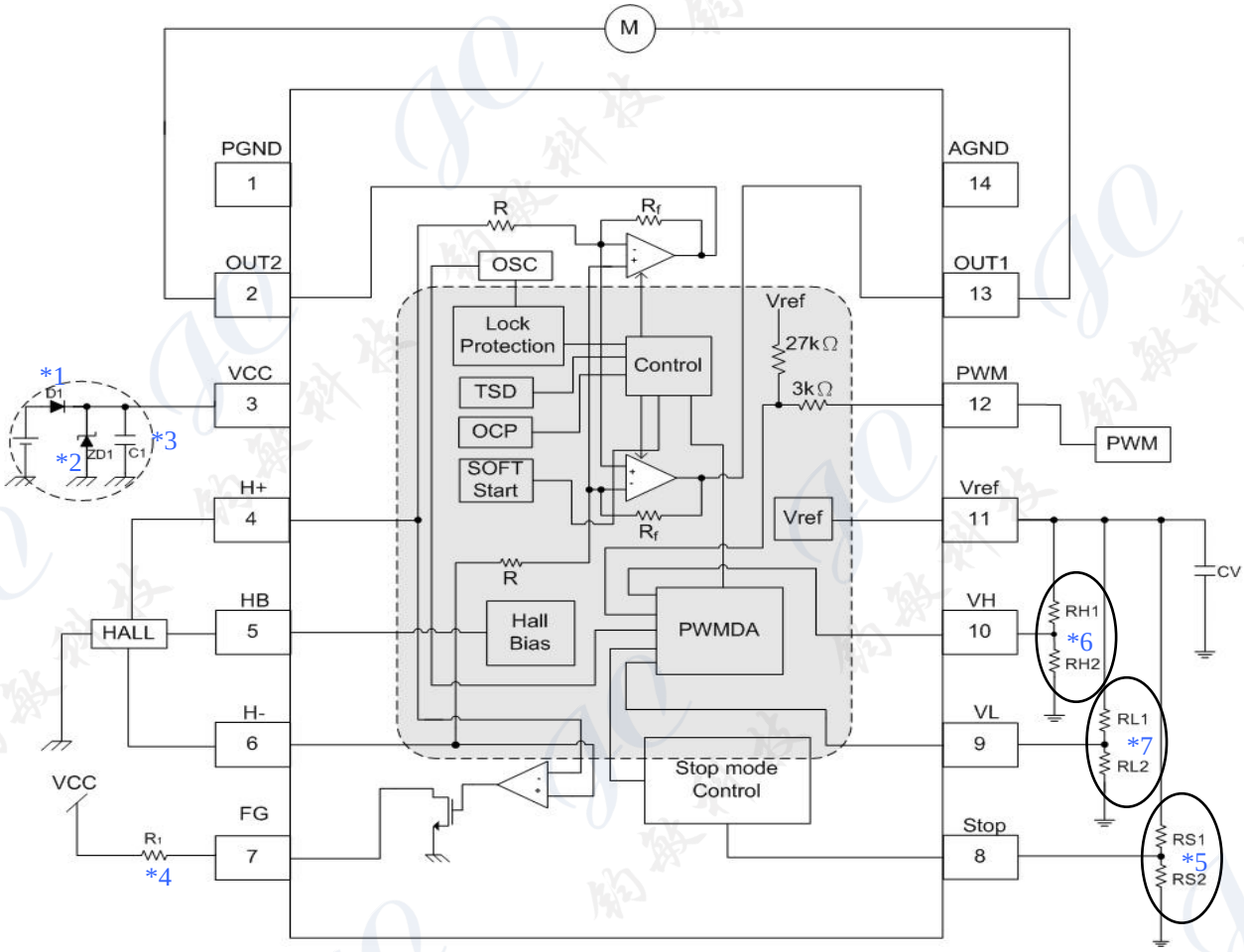


Fig2. Application circuit

1. Reverse connection of power supply may break the device. A countermeasure is needed such as using reverse current protection diode (D1) between power supply and V_{CC} terminal.

   The BEMF causes re-circulate current to power supply, when power-on or output changes. It may cause V_{CC} terminal to raise voltage, especially using reverse current protection diode (D1) because there is no way to return current back to power supply. In such case, please take necessary measures like below.

2. Connect a Zener diode (ZD1) between V_{CC} and GND terminal not to exceed the absolute maximum rating voltage.
3. Connect a capacitor (C1) between VCC and GND terminal to make a path of return current to power supply.
4. Open drain output. A pull-up resistances of 10kΩ should be inserted.

5. Stop Mode Control:
   When the IC using as Stop Mode control. The Stop Mode is setting by Stop pin, and Stop Duty can be adjusted by RS1 and RS2 ratio. The relation is shown as the Fig. 3 below. When not need this feature, set the Stop pin connected to Vref, avoid noise interference.

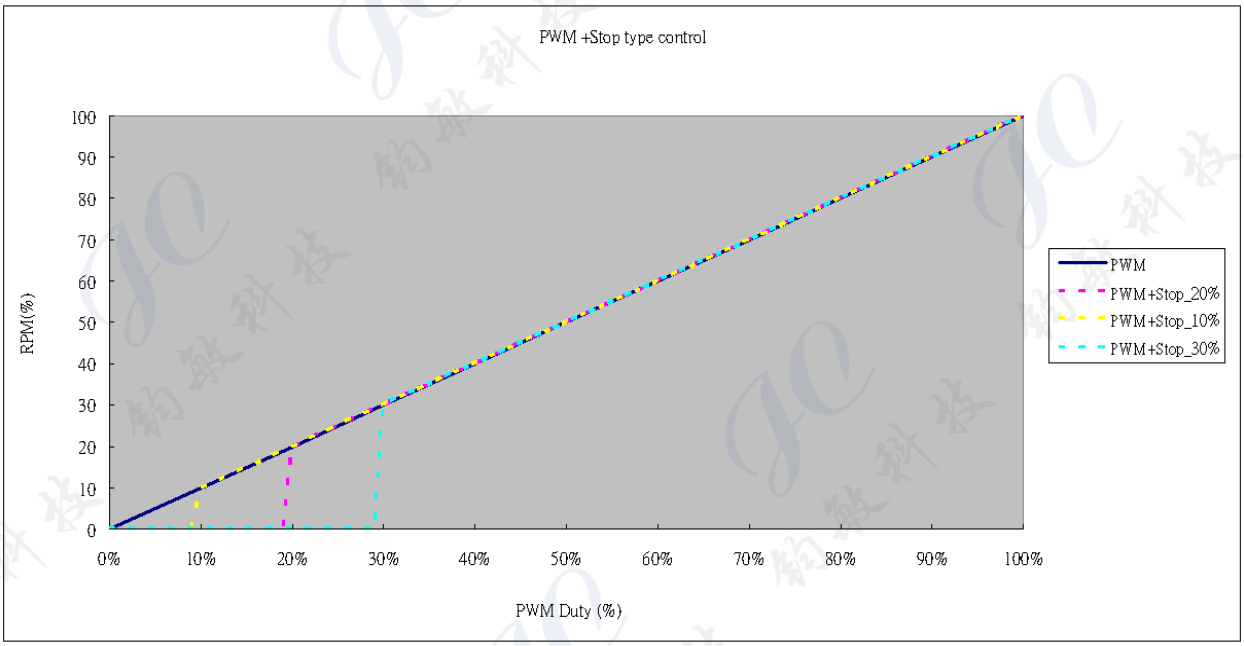


Fig.3 Stop mode control

6. Slope Low duty control:
   When the IC using as Slope low duty control. The low duty control is setting by VH pin, and low duty control can be adjusted by RH1 and RH2 ratio. Typical setting is 0.75VREF, The relation is shown as the Fig. 4 below.

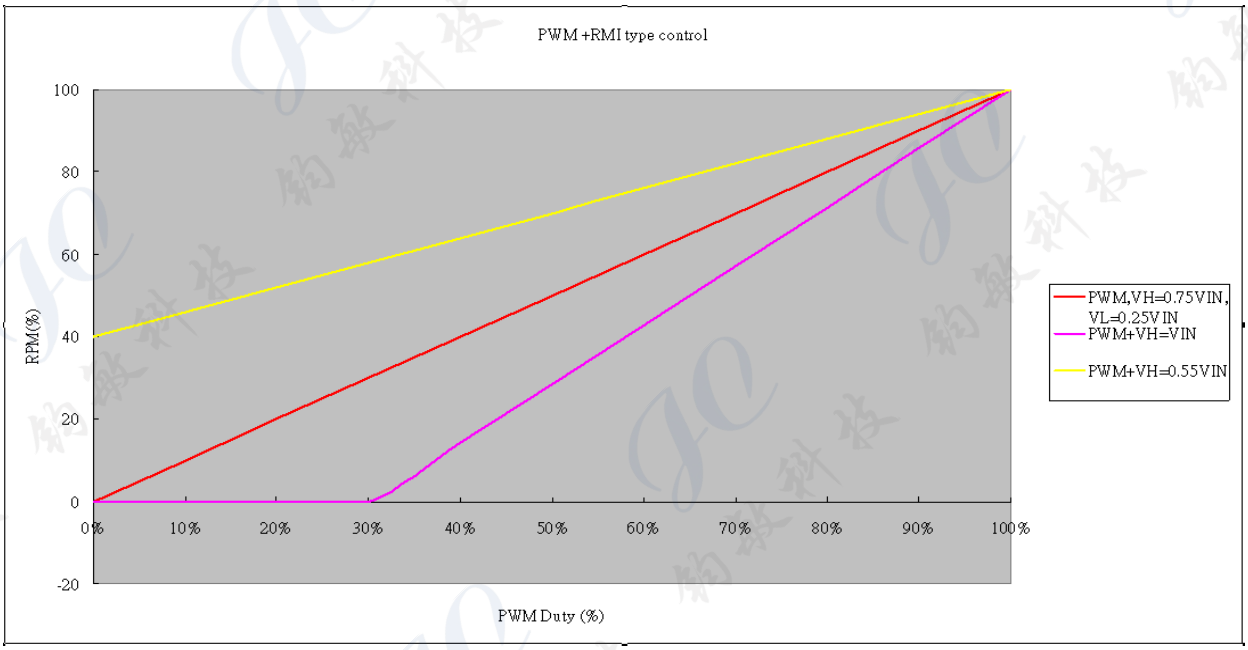


Fig.4 Slope low duty control

7. Slope Hi duty control:
   When the IC using as Slope Hi duty control. The Hi duty control is setting by VL pin, and Hi duty control can be adjusted by RL1 and RL2 ratio. Typical setting is 0.25VREF. The relation is shown as the Fig. 5 below.

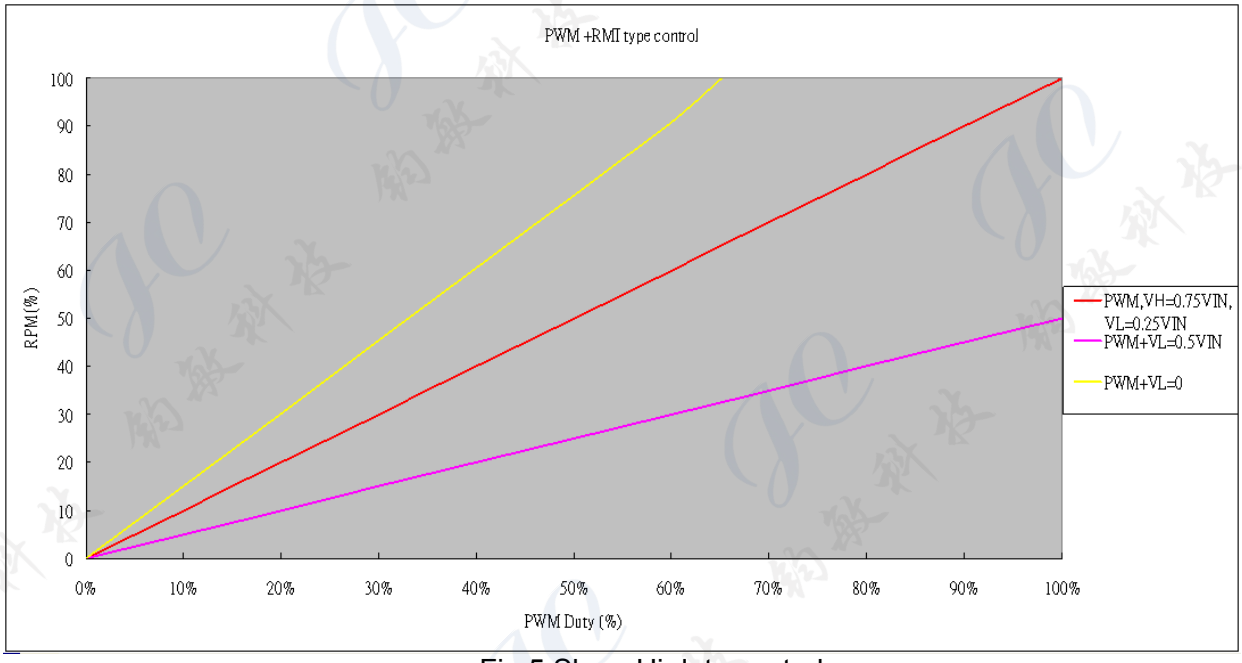


Fig.5 Slope Hi duty control

8. When PCB Layout, PGND & AGND (PIN 1 & Pin14) & E-PAD must be short-circuited to avoid noise.

Lock detection, automatic restart circuit

This IC detect the rotation of the motor by hall signal, and adjust lock detection ON time (Ton) and lock detection OFF time (Toff) by the internal counter. These time (Ton, Toff) are showed below.

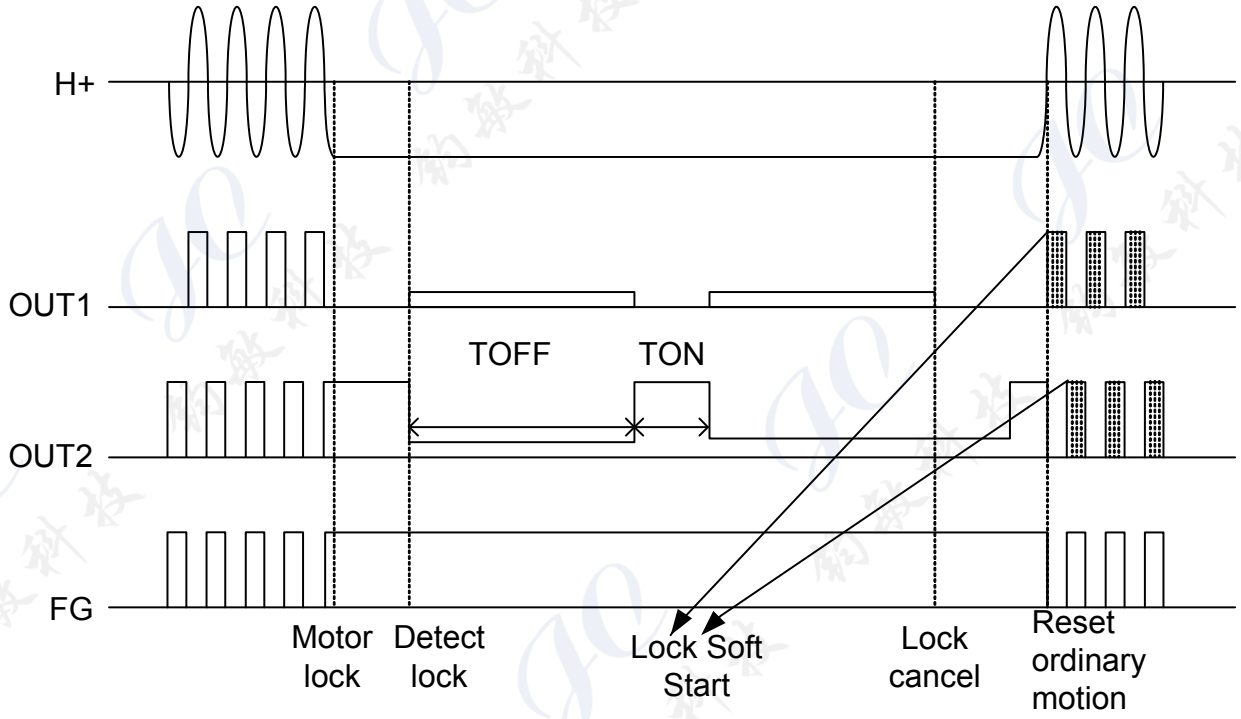


Fig.6 Lock detect and auto restart motion

Only in Lock detection ON Time (Ton), motor will be rest ordinary motion by switching over of hall signal. There is lock soft start function, When IC in reset ordinary motion, Output will shaping by 50% duty to start-up the motor, that will reduce lock start current and acoustic noise.

This IC make the lock protection function off, when the PWM input keeps low level for more than 70ms (typ.)

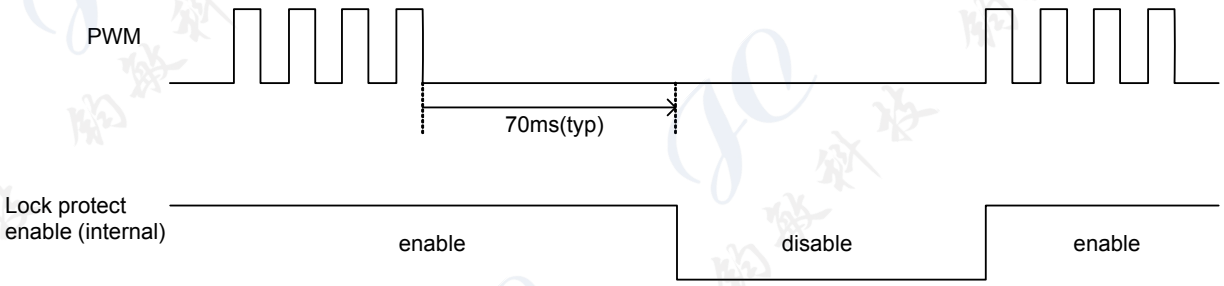


Fig.7 PWM input signal and lock protect function

Lock protect function does not work if PWM input frequency is slower than 15Hz (typ.)
So, please input faster frequency more than 20Hz

Soft switching function (silent drive setting)

Input signal to hall amplifier is amplified to produce an output signal.
When the hall element output signal is small, the gradient of switching of output waveform is gentle; When it is large on the contrary, the gradient of switching of output waveform is steep. Gain of 500 times (Typ.) is provided between input and output, therefore enter an appropriate hall element output to IC where output waveform swings sufficiently.

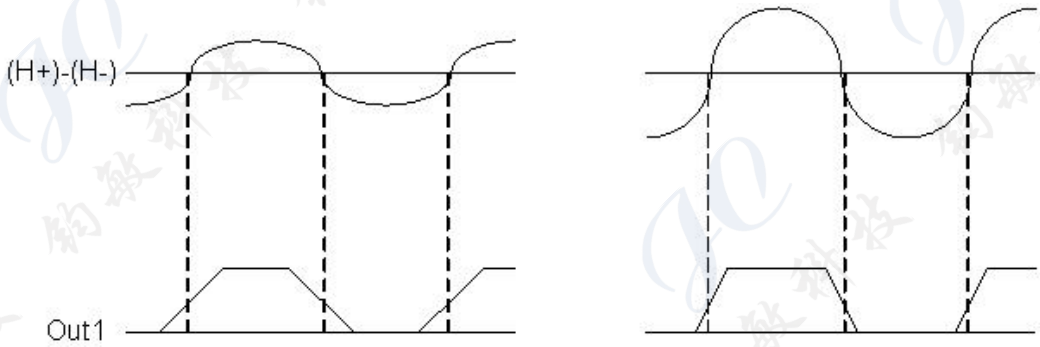


Fig.8 Relation between hall element output amplitude and output waveform

Hall input setting

Hall input voltage range is shown in operating conditions.

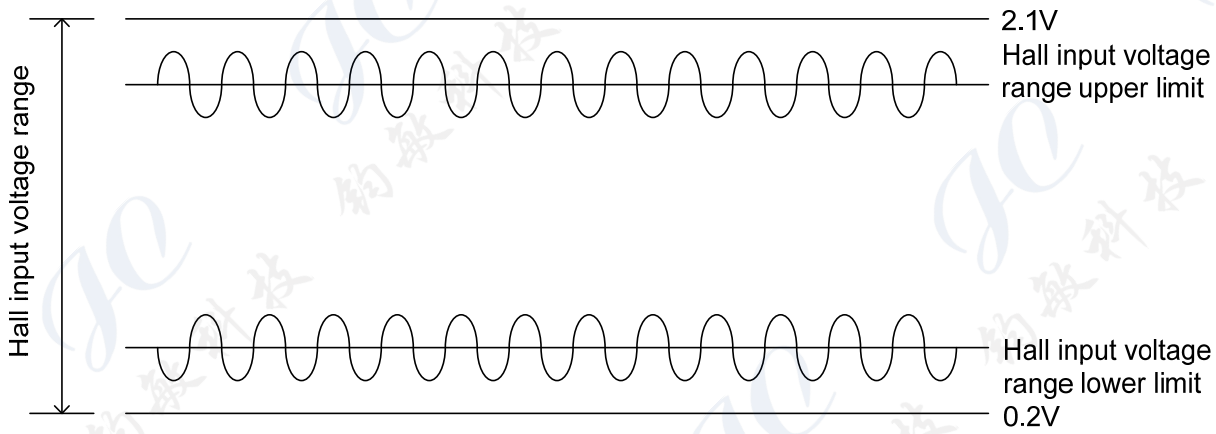


Fig.9 Hall input voltage range

Adjust the value of hall element bias resistor R1 in Fig.10 so that the input voltage of a hall amplifier is input in "hall input voltage range" including signal amplitude. Input out of the hall input voltage range may cause unexpected operation of output.

Reducing the noise of hall signal

Hall element may be affected by the depending on the wiring pattern of board. In this case, place a capacitor like C1 in Fig.10. In addition, when wiring from the hall element output to IC hall input is long, noise may be loaded on wiring. In this case, place a capacitor like C2 in Fig.10.

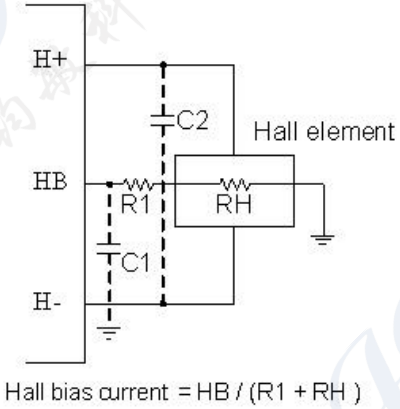


Fig.10 Application in the vicinity of hall signal

- **PWM input**

Rotation speed of motor can be changed by controlling ON/OFF of the upper output depending on duty of the signal input to PWM terminal.

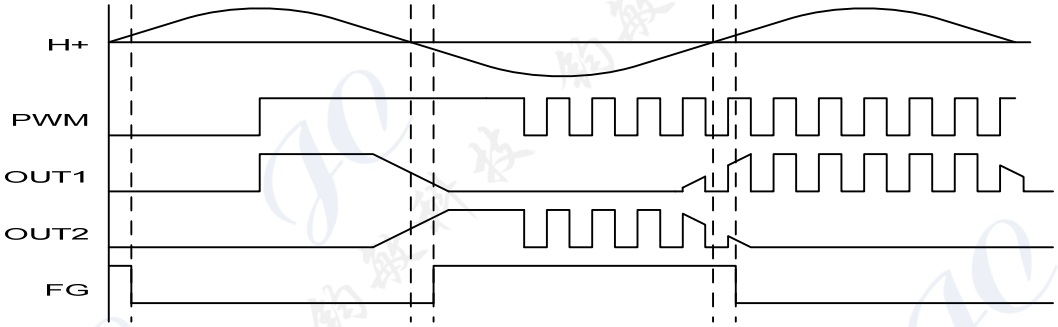


Fig.11 Timing chart in PWM control

When the voltage input to PWM terminal applies

H logic : normal operation
L logic : H side output is off

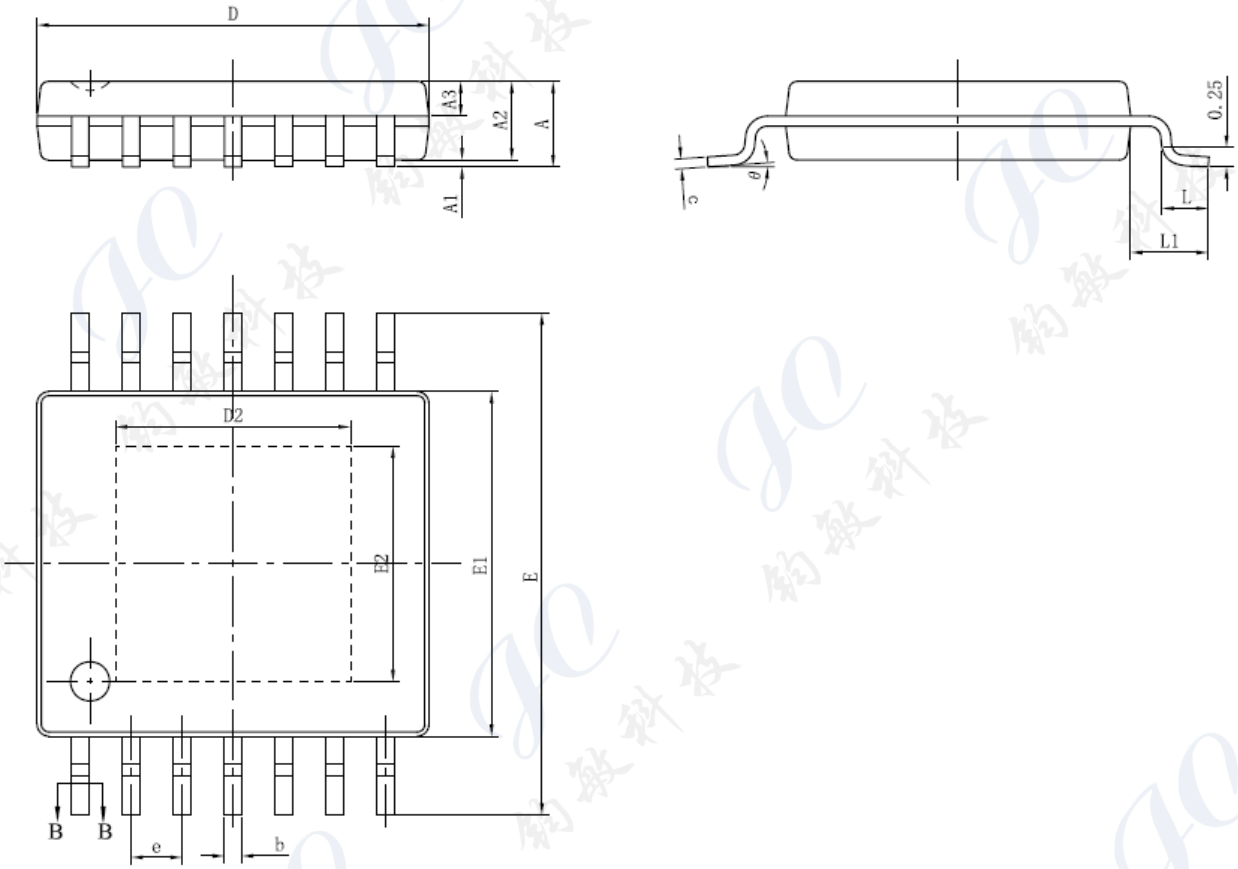
When PWM terminal is open, H logic is applied.
PWM terminal has hysteresis of 100mV (Typ.).

If H logic is applied to PWM terminal before Vcc voltage is applied to IC, current flows to Vcc terminal through ESD protection diode inside PWM terminal, resulting in malfunction may possibly occur.
When Vcc voltage is not apply to IC, do not apply voltage to PWM terminal.

Notes

1) Absolute maximum ratings
   This product is produced with strict quality control, but destroyed in using beyond absolute maximum ratings. Once IC destroyed, a failure mode cannot be defined (like short-mode or open-mode).Therefore, physical security counter measure, like fuse, is to be given when a specific mode to be beyond absolute maximum rating is considered.
2) Reverse connection of power supply
   Reverse connection of the power supply may break the device. A countermeasure is needed such as using reverse current protection diodes between the power supply and the V_{CC} terminal.
3) Power supply line
   The BEMF causes re-circulate current to power supply, Please connect a capacitor between power supply and GND as a route of re-circulate current. And please determine the capacitance after confirmation that the capacitance does not causes any problems.
4) GND potential
   The GND terminal should be the location of the lowest voltage on the chip.
5) Thermal design
   The thermal design should allow enough margin for actual power dissipation.
6) Mounting failures
   Mounting failures, such as misdirection or miss-mounts, may destroy the device.
   The electrical short caused by falling particle, between outputs; power supply and output; or output and ground, may damage the device.

- **Packaging outline --- eTSSOP 14L** **Unit : mm**



reference JEDEC MO229(D)VJGD-2

SYMBOL	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	-	1.2	-	0.047
A1	0.05	0.15	0.002	0.006
A2	0.9	1.05	0.035	0.041
A3	0.39	0.49	0.015	0.019
b	0.2	0.3	0.008	0.012
c	0.13	0.19	0.005	0.007
D	4.86	5.06	0.190	0.197
E1	4.3	4.5	0.168	0.176
E	6.2	6.6	0.242	0.257
D2	2.9	3.1	0.113	0.121
E2	2.9	3.1	0.113	0.121
L	0.45	0.75	0.018	0.029
L1	1.00BSC		0.039 BSC	
e	0.65 BSC		0.026 BSC	

Condition of Soldering

1).Manual Soldering

Time / Temperature ≤ 3 sec / 400 ± 10 °C （2 Times）

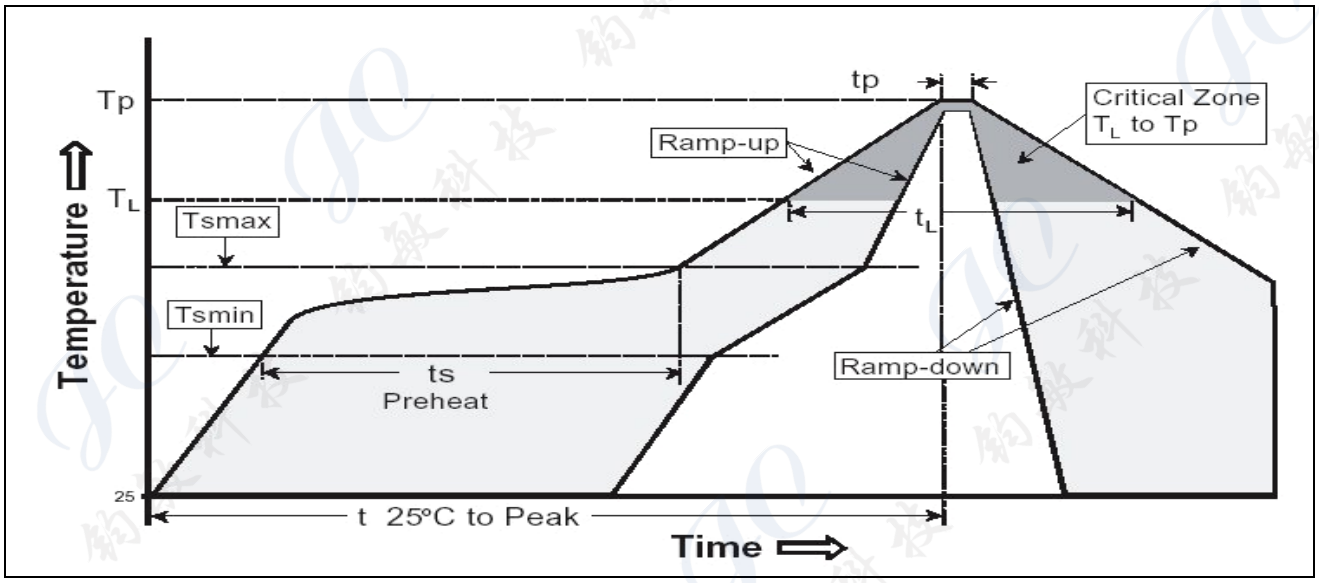
Test Results：0 fail/ 22 tested

Manual Soldering count：2 Times

2).Re-flow Soldering (follow IPC/JEDEC J-STD-020D)

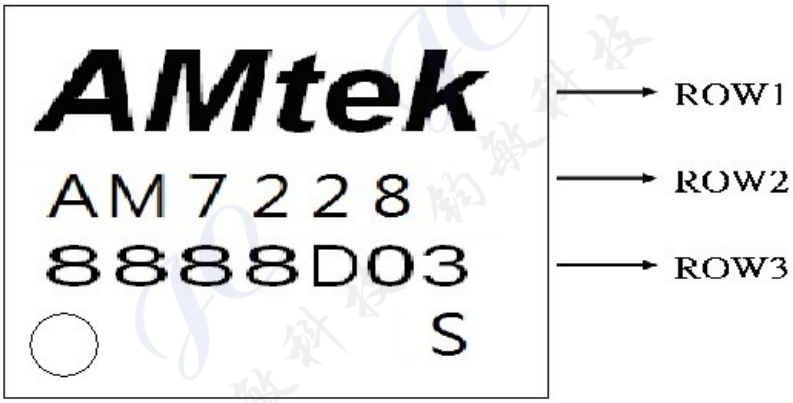
Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.
Preheat - Temperature Min (Ts min) - Temperature Max (Ts max) - Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ts max to T_L - Temperature Min (Ts min)	 3°C/second max.
Time maintained above: - Liquid us temperature (T_L) - Time (t_L) maintained above TL	 217°C 60-150 seconds
Peak package body temperature (Tp)	260 +0/-5°C
Time with 5°C of actual Peak - Temperature (tp)	30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



Test Results：0 fail/ 32 tested　Reflow count：3 cycles

- **Marking Identification**



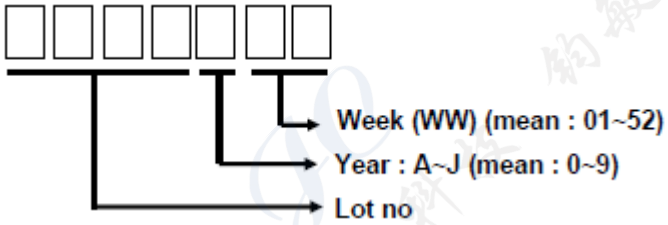
Row 1

AMtek

Row 2

Part number

Row 3



Week：Assembly Date Code

Year：Assembly Year

(Year_A=0,B=1,C=2,D=3,E=4,F=5,G=6,H=7,I=8,J=9, exp 2012=C)

Lot no：Wafer Lot No