DESCRIPTION

The PT5620 is a high-speed 100V single-phase gate driver for power MOSFET and IGBT devices with independent high and low side referenced output channels. Built-in dead time protection prevent damage to the half-bridge. The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. A novel high-voltage BCD process and common-mode noise canceling technique provide stable operation of high-side drivers under high dV/dt noise conditions while achieving excellent negative transient voltage tolerance. An enable pin (EN) is included so that standby mode may be used to set the chip into a low quiescent current state to realize long battery lifetime.

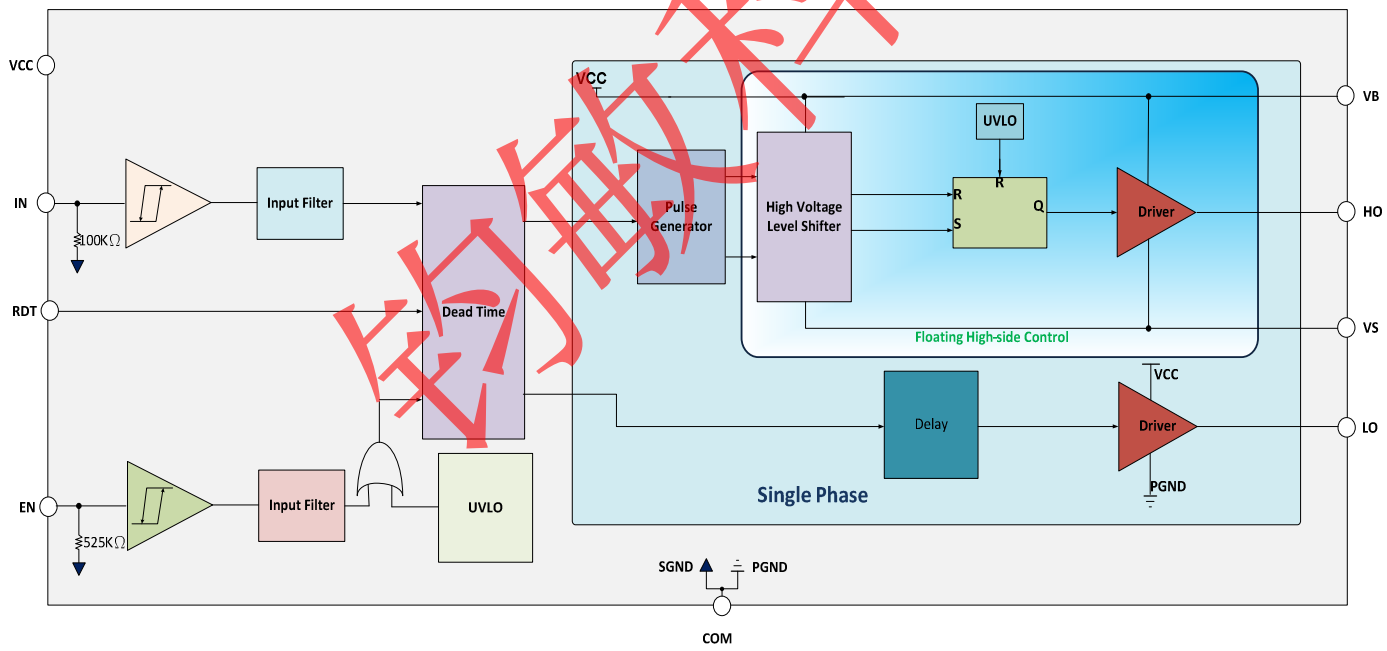
FEATURES

- Integrated 100V half-bridge high side driver
- Built-in dead time protection
- Under voltage lockout for VCC and VBS
- Low operation voltage 0–5.5V for VCC and VBS
- 3.3V and 5V input logic compatible
- Enable pin (EN) for low standby current
- IO+/IO-: +1.5A/–2.5A at VCC=15V, VBS=15V
- Dead time adjustment by RDT pin
- Common-mode dV/dt noise cancellation circuit
- Tolerant of negative transient voltage
- –40ºC to 125ºC operating range
- Small footprint package：MSOP10L、DFN8(3X3)、DFN10(3X3)

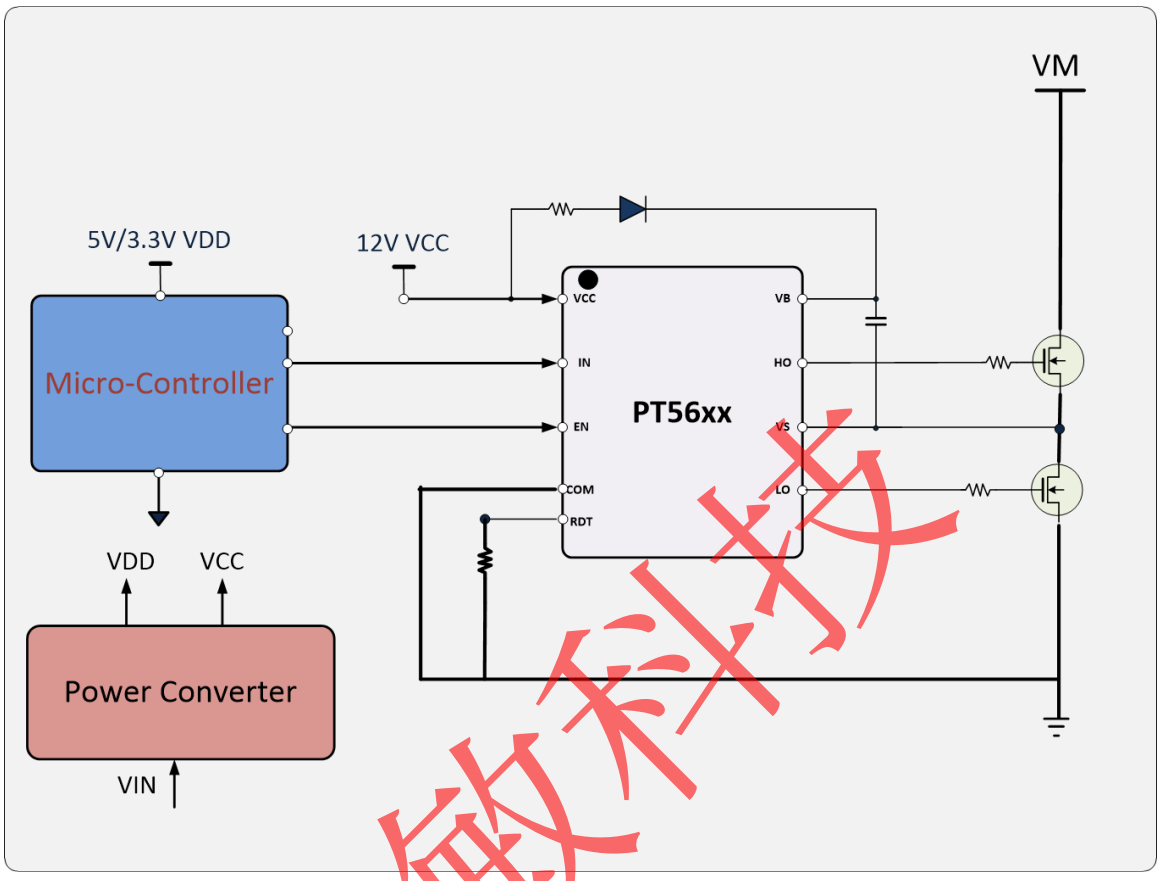
APPLICATION

- Wireless charging
- Half bridge/full bridge converters

BLOCK DIAGRAM

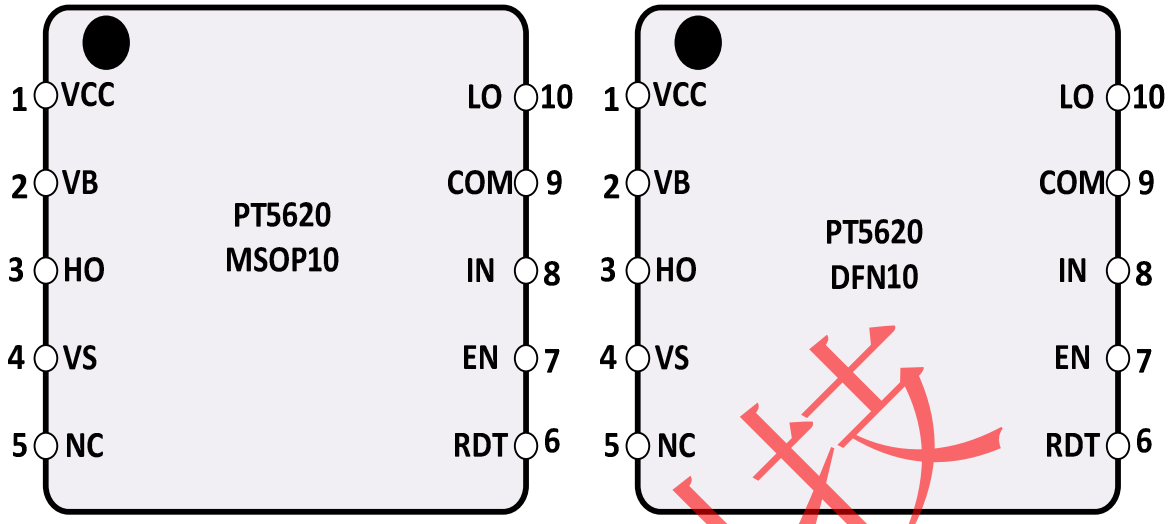


TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

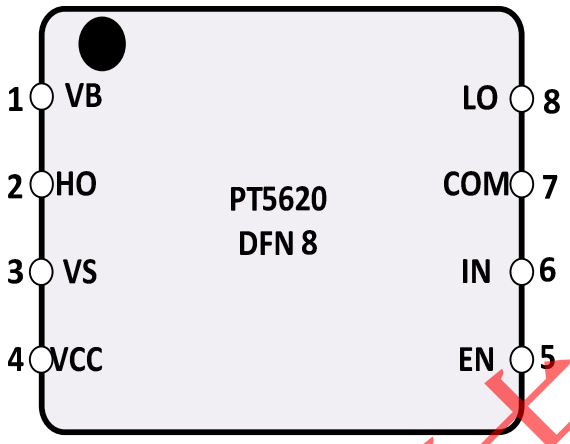
MSOP10L PACKAGE



PIN DESCRIPTION

Pin Name	Description	Pin No. MSOP10L /DFN10L
VCC	Logic and low-side gate drivers power supply voltage	1
VB	High-side driver floating supply	2
HO	High-side driver output	3
VS	High-side driver floating supply offset voltage	4
NC	Not connected	5
RDT	Connect the resistor to adjust dead time	6
EN	Logic input for enable mode control	7
IN	Logic input for gate driver input	8
COM	Logic ground and low-side gate drivers ground	9
LO	Low-side gate driver output	10

DFN8 PACKAGE



PIN DESCRIPTION

Pin Name	Description	Pin No.
		DFN8
VB	High-side driver floating supply	1
HO	High-side driver output	2
VS	High-side driver floating supply offset voltage	3
VCC	Logic and low-side gate drivers power supply voltage	4
EN	Logic input for enable mode control	5
IN	Logic input for gate driver input	6
COM	Logic ground and low-side gate drivers ground	7
LO	Low-side gate driver output	8

FUNCTION DESCRIPTION

LOW SIDE POWER SUPPLY: VCC

VCC is the low side supply which provides power to both input logic and low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than V_{CCUV+}=3.88V is present, as shown in FIG. 1. The PT5620 shuts down all gate driver outputs when the VCC supply voltage is below V_{CCUV-}=3.66 V, shown as FIG. 1. This prevents the external power devices from extremely low gate voltage levels during on-state which may result in excessive power dissipation.

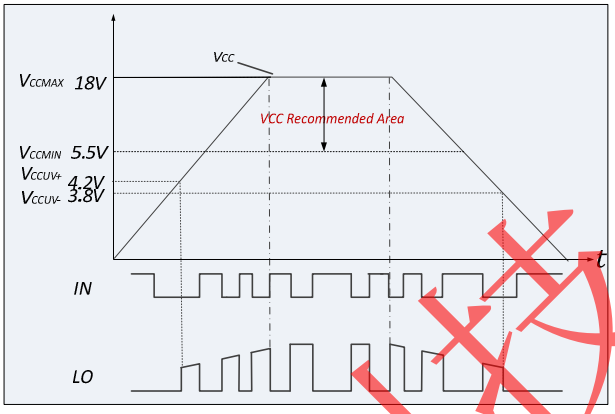


FIG. 1 VCC supply UVLO operating area

HIGH SIDE POWER SUPPLY: VBS

VBS is the high side supply voltage. The total high side circuitry may float with respect to COM following the external high side power device emitter/source voltage. Due to the internal low power consumption, the entire high side circuitry may be supplied by a bootstrap topology connected to VCC and may be powered with small bootstrap capacitors. The device operating region as a function of the supply voltage is given in FIG. 2.

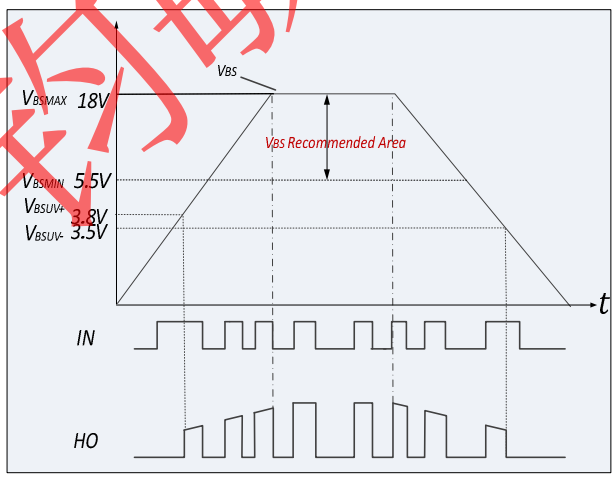


FIG. 2 VBS supply UVLO operating area

LOW SIDE AND HIGH CONTROL INPUT LOGIC: VIN

The Schmitt trigger threshold of each input is designed low enough to guarantee LSTTL and CMOS compatibility with 3.3V controller outputs. Input Schmitt triggers and advanced noise filtering provide noise rejection of short input pulses. An internal pull-down resistor of about 100kΩ (positive logic) pre-biases each input during the VCC supply start-up state.

DEAD TIME PROTECTION

The PT5620 includes an adjustable dead time protection circuit. The amount of dead time delay is set by the resistance on the RDT pin. The dead time feature inserts a time delay (a minimum dead time) during which both the high- and low-side power switches are turned off. This is done to ensure that one power switch has fully turned off before the other power switch is turned on. FIG. 3 illustrates the dead time period and the relationship between the power switch control signals.

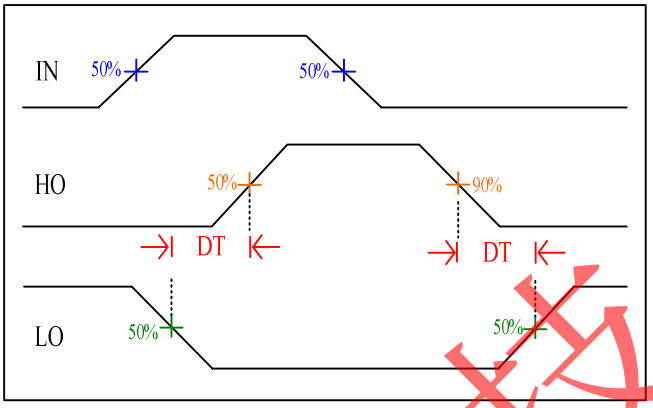


FIG. 3 Dead time protection

STANDBY MODE

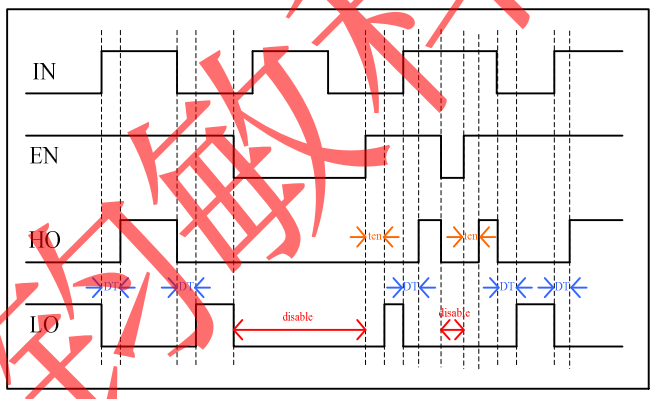


FIG. 4 Logic operation

The PT5620 packaged in MSOP10 provides an enable pin (EN) to allow the device to work in a low current dissipation state. The EN pin is compatible with 3.3/5V logic levels. If EN is set to logic LOW, the device is forced into standby mode and all gate driver outputs are locked into a logic LOW state and only 5μA (typ.) is dissipated, as shown in FIG. 4. If EN goes from logic LOW to logic HIGH and incorporates a delay of 4.6μs (typ.), the device may be released from standby mode and all outputs are enabled. In order to lower the bias current, a sufficiently large resistor (525kΩ) is tied between ENB and COM.

GATE DRIVER (HO, LO)

High side and low side driver outputs are specifically designed for pulse operation and dedicated to driving power devices such as IGBTs and power MOSFETs. High and low side outputs are state triggered by the rising and falling edges of the IN pin, as shown in FIG. 4. After releasing from an under-voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output. In contrast, after releasing from an under-voltage condition of the VCC supply, the low side outputs may directly switch to the state determined by their respective inputs without the additional constraints required by the high side driver.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or cause abnormal function. All the voltage parameters are absolute voltages referenced to IC COM unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	V_B	–0.3	100	V
High-side offset voltage	V_S	V_B–20	V_B+0.3	
High-side gate driver output voltage	V_{HO}	V_S–0.3	V_B+0.3	
Low-side gate driver output voltage	V_{LO}	COM–0.3	V_{CC}+0.3	
Logic input voltage	V_{IN} EN	–0.3	20	
Low-side supply voltage	V_{CC}	–0.3	20	
Thermal resistance，junction to ambient ①	Rth_{JA}	—	MSOP10:120	°C /W
Allowable offset voltage slew rate	dV/dt	—	50	V/ns
Junction temperature	T_J	–40	+150	°C
Storage temperature	T_S	–40	+150	
Soldering lead temperature (duration 10s)	TL	—	260	°C

Note:
①: P_D and Rth_{JA} are only guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Low-side supply voltage	V_{CC}	5.5	—	18	V
High-side floating supply offset voltage②	V_S	COM-6	—	60	
High-side floating supply voltage	V_B	V_S+5.5	—	V_B+18	
High-side gate driver output voltage	VHO	V_S	—	V_B	
Low-side gate driver output voltage	V_{LO}	COM	—	V_{CC}	
Logic input voltage	V_{IN} EN	0	—	5	
IC operating junction temperature	T_J	–40	—	+125	°C

②: For V_{BS}=15V, normal logic operation for Vs is between COM–6V to 100V. High-side circuitry will sustain current state if VS is between COM–6V to COM–V_{BS}. The parameter is only guaranteed by design.

STATIC ELECTRICAL CHARACTERISTICS

(V_{CC}–COM)=(V_B–V_S)=15V, V_{EN}=5V, RDT=100KΩ. Ambient temperature T_A=25ºC unless otherwise specified. The $V_{IN,TH}$, V_I, and I_{IN} parameters are referenced to COM and are applicable to all channels. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
Quiescent VCC supply current	I_{QVCC1}	V_{IN}=0 or 5V,	210	425	680	μA
Quiescent VCC supply current in standby mode	I_{QVCC2}	V_{IN}=0 or 5V,	—	7	60	
operating VCC supply current	I_{VCCOP}	f_{IN}=20KHz	—	650	—	
VCC supply under-voltage positive going threshold	V_{CCUV+}	—	2.9	3.88	5.5	V
VCC supply under-voltage negative going threshold	V_{CCUV-}	—	2.5	3.66	5.1	
VCC supply under-voltage lockout hysteresis	V_{CCHYS}	—	—	0.22	—	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}	—	2.5	3.6	5.5	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}	—	2.2	3.4	4.8	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$	—	—	0.2	—	
High side quiescent VBS supply current	I_{QBS}	V_{BS}=15V	25	50	75	μA
Offset supply leakage current	I_{LK}	V_B=V_S=100V V_{CC}=0V	—	—	10	
Logic Input Section						
Logic HIGH input voltage IN and EN	V_{IH}	—	2.5	—	—	V
Logic LOW input voltage IN and EN	V_{IL}	—	—	—	0.8	
Input positive going threshold	$V_{IN,TH+}$	—	—	1.9	—	
Input negative going threshold	$V_{IN,TH-}$	—	—	1.4	—	
Logic HIGH input bias current	I_{IN+}	V_{IN}=5V	—	50	—	μA
Logic LOW input bias current	I_{IN-}	V_{IN}=0	—	0	—	
Gate Driver Output Section						
High side output HIGH short-circuit pulse current	I_{HO+}	V_{HO}=V_S=0	—	1.5	—	A
High side output LOW short-circuit pulse current	I_{HO-}	V_{HO}=V_B=15V	—	2.5	—	
Low side output HIGH short-circuit pulse current	I_{LO+}	V_{LO}=0	—	1.5	—	
Low side output LOW short-circuit pulse current	I_{LO-}	V_{LO}=V_{CC}=15V	—	2.5	—	
Allowable negative VS voltage for HIN1,2,3 signal propagation to HO1,2,3	V_{SN}	V_{BS}=15V	—	–10	—	V

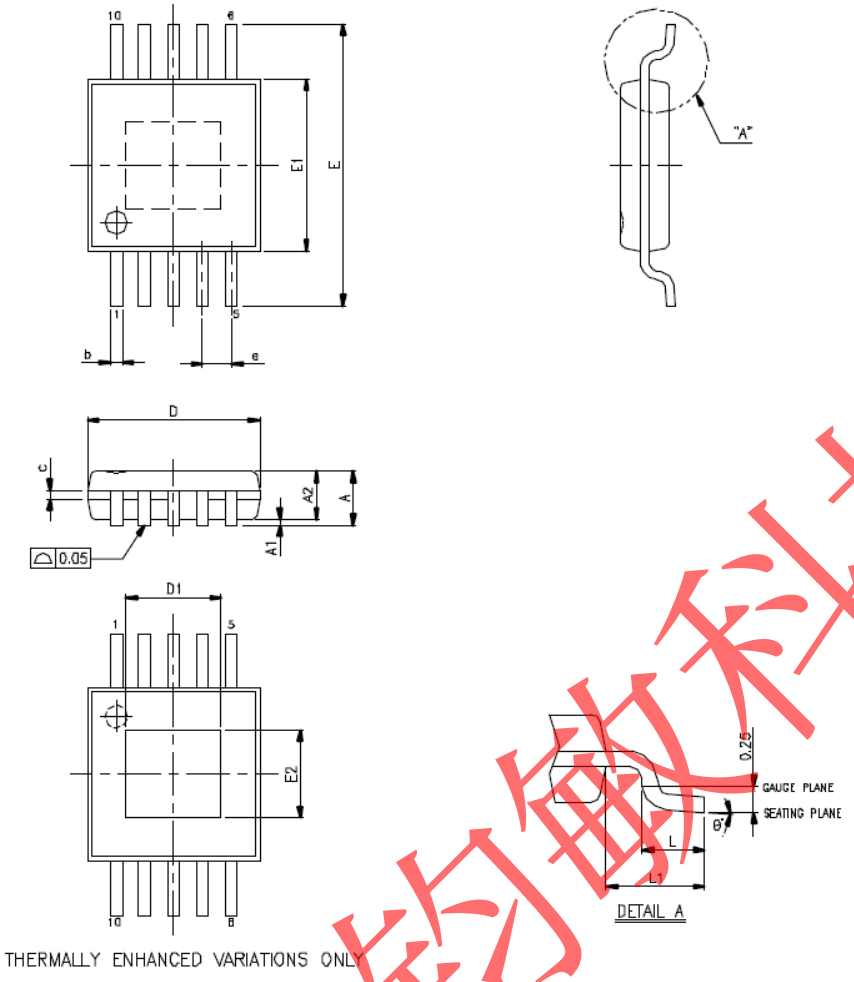
DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{CC}–COM)=(V_B–V_S)=15V, V_{EN}=5V, RDT=100KΩ, V_S=COM, and C_{load}=1nF unless otherwise specified, ambient temperature T_A=25ºC.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	t_{on}	V_{IN}=5V, V_S=0	—	350	—	ns
Turn-off propagation delay	t_{off}	V_{IN}=0, V_S=0	—	110	—	
Turn-on rise time	t_r	V_{IN}=5V, V_S=0	—	26	—	
Turn-off fall time	t_f	V_{IN}=0, V_S=0	—	25	—	
Dead time	DT	RDT=0Ω, V_{IN}=0V and 5V	—	32	—	
		RDT=10KΩ, V_{IN}=0V and 5V	—	55	—	
		RDT=30KΩ, V_{IN}=0V and 5V	—	135	—	
		RDT=50KΩ, V_{IN}=0V and 5V	—	180	—	
		RDT=100KΩ, V_{IN}=0V and 5V	—	295	—	
		RDT=150KΩ, V_{IN}=0V and 5V	—	410	—	
		RDT=open	—	7700	—	
max current of RDT Pin	IRDT_max	RDT=0Ω	0.75	1	1.25	mA
EN input filter time	$t_{FLT,EN}$	V_{EN}=0 and 5V	—	400	—	ns
EN input logic HIGH to HO/LO turn-off delay time	$t_{off,EN}$	V_{EN}=0V	—	0.55	—	μs
EN input logic LOW to HO/LO turn-on delay time	$t_{on,EN}$	V_{EN}=5V	—	5.2	—	

PACKAGE INFORMATION

10 PINS, MSOP, 118MIL



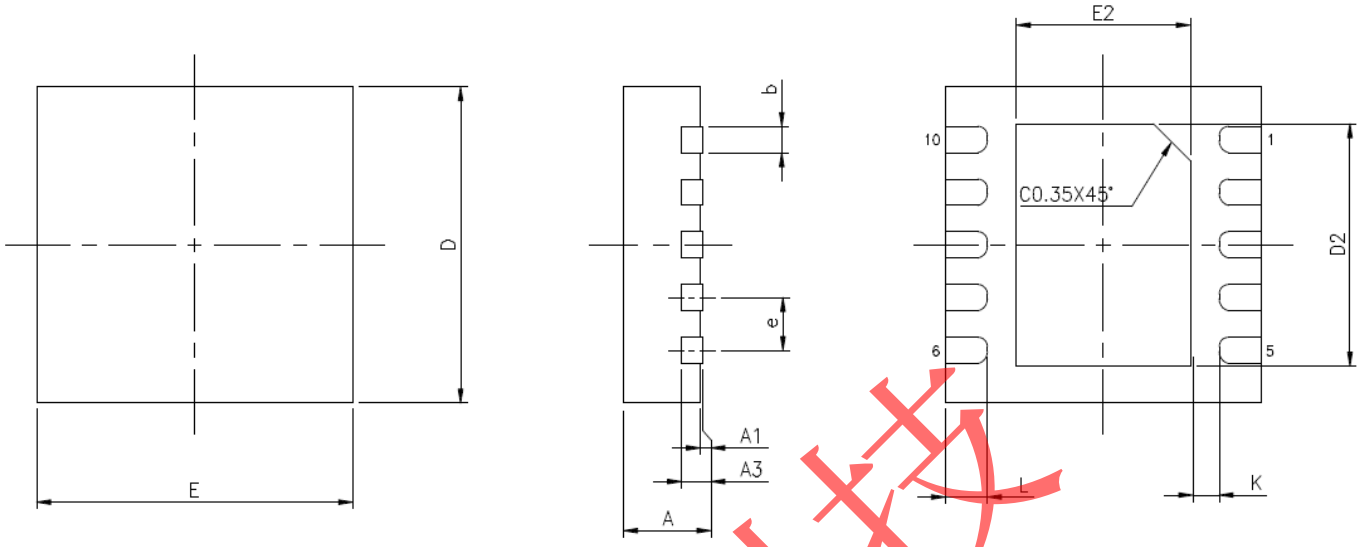
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
b	0.17	–	0.27
c	0.08	–	0.23
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
e		0.50 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

PACKAGE MARKING AND ORDERING INFORMATION:

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
PT5620	PT5620	10 Pins, MSOP, 118mil	Tape and Reel	-	-	-

10 PINS, DFN, 3X3 MM



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D2	2.20	—	2.70
E2	1.40	—	1.75
e		0.50 BSC.	
L	0.30	0.40	0.50
K	0.20	—	—

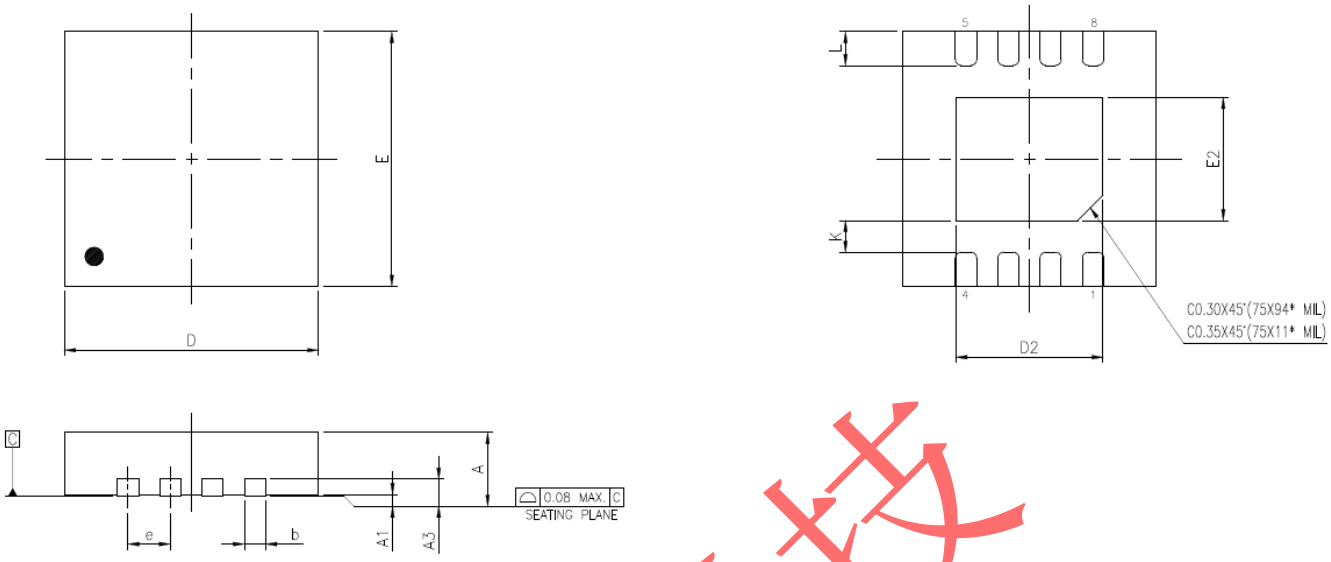
UNIT : mm

NOTES :
1. JEDEC OUTLINE : MO-229 WEED-5.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PACKAGE MARKING AND ORDERING INFORMATION:

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
PT5620	PT5620	10 Pins, DFN, 3x3 MM	Tape and Reel	-	-	-

8 PINS, DFN, 3X3 MM



	PACKAGE TYPE					
JEDEC OUTLINE	MO-229			MO-229		
PKG CODE	WDFN(X309)			VDFN(Y309)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30
D	3.00 BSC			3.00 BSC		
E	3.00 BSC			3.00 BSC		
e	0.50 BSC			0.50 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠ 75X94* MIL	1.69	1.74	1.79	1.40	1.45	1.50	V	X	N/A
⚠ 75X11* MIL	2.35	2.40	2.45	1.65	1.70	1.75	V	X	(W)V3030D-4

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

PACKAGE MARKING AND ORDERING INFORMATION:

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
PT5620	PT5620	8 Pins, DFN, 3x3 MM	Tape and Reel	-	-	-

IMPORTANT NOTICE

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REVISION HISTORY

Date	Revision No.	Reference No.	Modification
2018-06-29	PT5620 REF1.0.doc		Initial Version
2018-09-29	PT5620 REF1.1.doc		Modify the value of VCC and VBS from 12 to 15V. Modify the “Static ELECTRICAL CHARACTERISTICS”. Modify “PIN CONFIGURATION and PACKAGE INFORMATION”